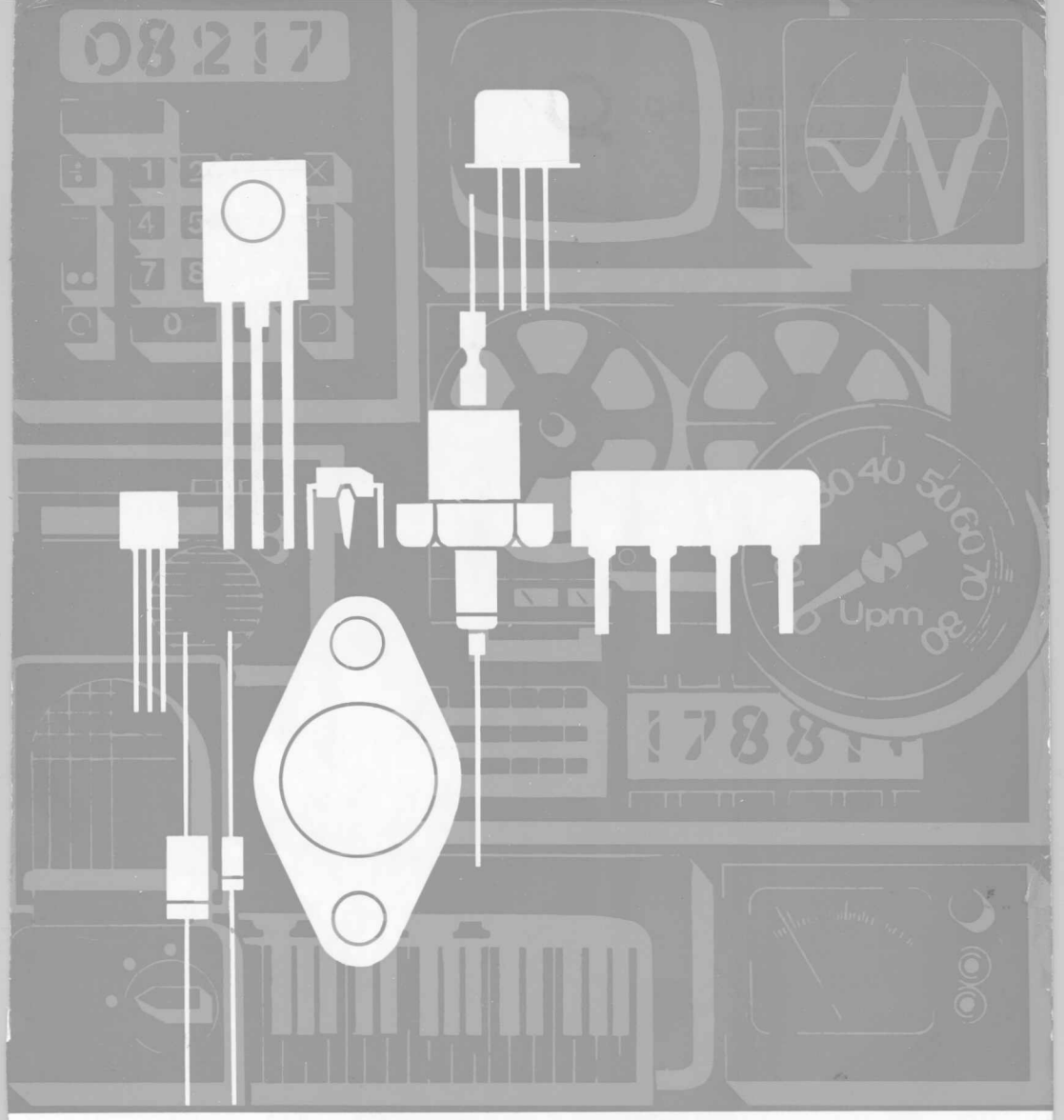

Discrete Semiconductor Circuit Examples

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Discrete Semiconductor Circuit Examples

Manual 1973

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Preface

This book is a revised version of an earlier collection of circuit examples to which new ones, devised in the INTERMETALL application laboratory, have been added. It does not contain any RF circuits or circuits with thyristors, four-layer diodes or integrated devices. Simple circuits, which allow basic principles and their elaborations to be recognized, have been chosen rather than complex ones. For the sake of clarity, power supplies have been omitted on most of the diagrams.

The explanatory text represents a compromise in that it had to be written so as to provide a coherent book as well as a reference manual divided into self-contained sections. Whilst there are frequent references to other circuits in the book, this does not mean that lengthly passages have to be read in order to understand a particular circuit. The descriptions of circuits with which familiarity can be assumed are kept brief (unless they are of special importance), whilst those of lesser known and novel ones are treated in greater depth. Most circuit diagrams contain detailed component information; design procedures are given only for very simple circuits.

As far as the lay-out of the circuit diagrams is concerned, an attempt has been made to adhere to the following: The top and bottom limits of each diagram are formed by the two supply lines; the component networks are then drawn between these lines so that physical position in the diagram is indicative of potential. For example, if a circuit employs mainly NPN transistors, then the positive line is near the top of the page and the top terminals of any components drawn in a vertical position would be more positive than the bottom ones; the opposite applies to circuits incorporating PNP transistors. However, this rule is not always strictly observed for the sake of even component distribution and space utilization.

Circuits designed for NPN transistors will, in general, also function with PNP devices, provided the polarity of the supply and that of any electrolytics and diodes is reversed.

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I. Voltage and Current Stabilizers

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Basic Zener Diode Shunt Stabilizer

A stabilizer, in its simplest form, consists of a resistor R in series with a zener diode, this network being connected to the unstabilized input voltage V_{in}. The stabilized output voltage V_{out} is taken from across the zener diode. If the output current I_{out} decreases, then I_Z, the operating current through the diode, increases by nearly the same amount, with the result that the output voltage is held approximately constant. If, on the other hand, the input voltage increases, then I_Z, and hence the voltage drop across R, increase sufficiently to compensate for the increase in input voltage.

The stabilizing factor S is the ratio of relative input voltage change to relative output voltage change:

$$S = \frac{dV_{in}/V_{in}}{dV_{out}/V_{out}}$$

or, for high values of R,

$$S \approx \frac{R}{r_z} \cdot \frac{V_{out}}{V_{in}}$$

The differential output resistance of the stabilizer is approximately the same as r_z, the differential resistance of the zener diode.

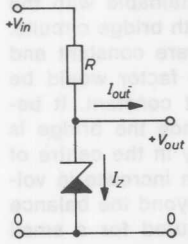
The value of resistor R is governed by two factors, namely on the one hand by the maximum current which the diode can handle without suffering damage, and on the other by the lowest diode reverse current necessary to ensure reliable breakdown conditions.

The following rules apply:

$$R > \frac{V_{in\ max} - V_{out}}{I_{Z\ max} + I_{out\ min}}$$

$$R < \frac{V_{in\ max} - V_{out}}{I_{Z\ min} + I_{out\ max}}$$

where $I_{Z\ max}$ is the maximum permissible operating current quoted in the relevant data sheet, and $I_{Z\ min}$ is the minimum current which can be tolerated without increasing the differential resistance above an acceptable limit. I_Z should be approcimately 5 to 10 % of $I_{Z\ max}$.



1. Basic zener diode shunt stabilizer

Zener Diode Bridge Stabilizers

Considerably better stabilization factors than those attainable with the basic zener diode circuit of Fig. I. 1. can be obtained with bridge circuits. In fact, if r_z, the differential zener diode resistance, were constant and the bridge accurately balanced, then the stabilization factor would be infinite. Unfortunately the differential resistance is not constant. It becomes smaller as the diode current is increased. Hence the bridge is usually adjusted so that balance conditions obtain only in the centre of the desired operating range. Under these conditions an increase in voltage causes the output to increase initially, and then, beyond the balance point, to decrease. If the stabilization factor is measured for a small input voltage swing about a mean input voltage, it will be found that, as the mean input voltage is varied from low to high values, S is initially positive and increases until the balance point is reached when it becomes $+\infty$; S then changes sign and slowly decreases in magnitude from $-\infty$ downwards.

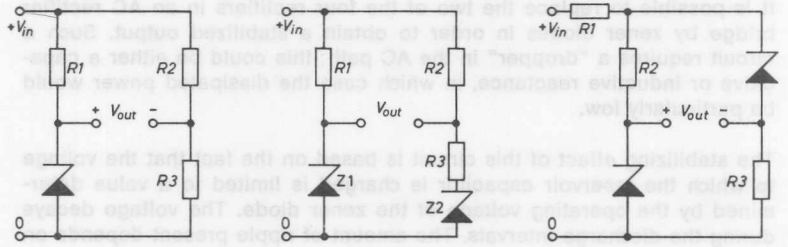
If the stabilization factor is measured by determining the ratio of maximum input change to maximum output change and the signs are disregarded, then, for the usual $\pm$ 10% input variation, a stabilization factor of the order of several hundred can be expected.

To balance the bridge, an AC voltage should be superimposed on the DC supply and the resistive bridge arms adjusted for minimum AC output.

A better balancing method, which also takes the thermal part of the differential zener diode resistance into account, is to switch the DC bridge input between two levels. In this case bridge output readings should be taken only after the circuit has reached thermal equilibrium.

a) The bridge comprises one zener diode and three resistors, the load being connected to the "detector" points. The resistance values should be chosen so that, with the bridge operating in the centre of the desired stabilization range, the condition $R1/r_z = R2/R3$ is fulfilled. The differential output resistance of this circuit is approximately $r_z + R3$; the output voltage is equal to the diode zener voltage minus the voltage dropped across $R3$.

b) This circuit is particularly suitable for use as a low voltage stabilizer, the output being approximately equal to $V_{Z1} - V_{Z2}$, where V_{Z1} and V_{Z2} are the operating voltages of the zener diodes Z1 and Z2 respectively. The differential output resistance is $r_{z1} + r_{z2} + R3$. The bridge should be balanced in the centre of the desired stabilization range so that $R1/r_{z1} = R2/(R3 + r_{z2})$. $R3$ can be omitted if a slight difference in the currents passed by the two bridge arms is acceptable, or if the differential resistance values of the two diodes are approximately equal.



2. Zener diode bridge stabilizers

c) This circuit is recommended when the difference between input and output voltage is only small. The operating voltages of the zener diodes should be closely matched; the same applies to the values of the resistors *R2* and *R3,* which should be chosen so that with the bridge operating in the centre of the stabilization range, they have the same value as the differential resistance of the zener diodes. The value of resistor *R1* should be low enough to ensure sufficient current flow through the diode at low input voltages, but not so low that at maximum input the zener diodes are overloaded.

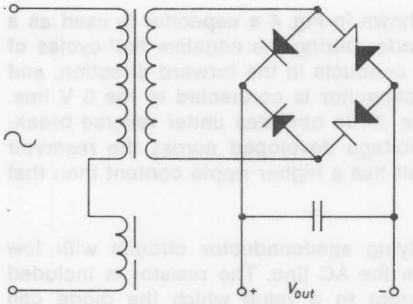
Rectifier Bridge Stabilizer

It is possible to replace the two of the four rectifiers in an AC rectifier bridge by zener diodes in order to obtain a stabilized output. Such a circuit requires a "dropper" in the AC path; this could be either a capacitive or inductive reactance, in which case the dissipated power would be particularly low.

The stabilizing effect of this circuit is based on the fact that the voltage to which the reservoir capacitor is charged is limited to a value determined by the operating voltage of the zener diode. The voltage decays during the discharge intervals. The amount of ripple present depends on the capacitance of the reservoir capacitor, the supply frequency and the load current. The circuit is, therefore, only suitable for use as a pre-stabilizer or semi-stabilized supply.

The voltage across the reservoir capacitor is limited to a peak value equal to the difference between the operating voltage of the zener diode and the forward voltage of the conventional diode. The operating voltages of the two zener diodes should be matched as closely as possible, otherwise the ripple content (at fundamental supply frequency) would be increased.

In the circuit shown in Fig. 3 a choke is used as an AC input dropper. Alternatively the supply transformer could be designed as a leakage-reactance transformer, in which case the choke could be omitted because the input current is then limited by the leakage reactance of the transformer.



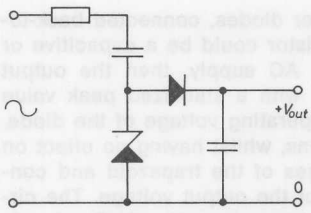
3. Rectifier bridge stabilizer

Half-Wave Rectifier Stabilizer

In the half-wave rectifier circuit shown in Fig. 4 a capacitor is used as a series "dropper" for the zener diode. During the negative half-cycles of the input voltage the zener diode conducts in the forward direction, and the lower terminal of the series capacitor is connected to the 0 V line. During the positive half-cycles the diode operates under reverse breakdown conditions and limits the voltage developed across the reservoir capacitor. The output of this circuit has a higher ripple content than that of a full-wave circuit.

The circuit is suitable for supplying semiconductor circuits with low current requirements directly from the AC line. The resistor is included to limit the capacitor inrush current to a value which the diode can handle safely.

It should be noted that the absence of an AC line transformer calls for special safety precautions.



4. Half-wave rectifier stabilizer

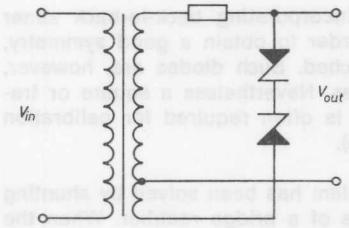
AC Stabilizer

If a network, comprising two identical zener diodes, connected back-to-back and in series with a resistor (this resistor could be a capacitive or inductive reactance), is connected to an AC supply, then the output waveform will be a symmetrical trapezoid with a stabilized peak value equal to the sum of the forward and the operating voltage of the diode. Note, however, that any input level variations, whilst having no effect on the peak value, will affect the sloping edges of the trapezoid and consequently the form factor and RMS value of the output voltage. The circuit is, therefore, only suitable for applications where the RMS value is unimportant (e. g. as a voltage calibrator in oscilloscopes).

The circuit can be modified to form a bridge by providing the transformer secondary with a tap (Fig. 5 a). At low input voltages the output then has the near-trapezoidal shape shown in Fig. 5 b, the input sine wave being clipped to V_B (the sum of forward and operating voltage); the effect of the "bucking" voltage presented across the lower part of the secondary winding is negligible in these circumstances.

Without the bucking voltage any large increase in input would result in what is virtually a square wave with a peak value of V_B. The RMS value of such a waveform would be considerably higher than that of the trapezoidal voltage shown in Fig. 5 b (which also has a peak value of V_B). However, the bucking winding now produces an opposing voltage (dotted line in Fig. 5 c) which, if the number of turns is correct, tends to keep the RMS value of the output voltage (thick lines) nearly constant.

One application for such a circuit would be as a filament voltage stabilizer for vacuum tubes used in precision measurement equipment.



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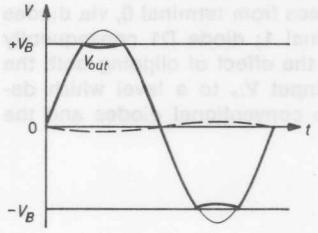

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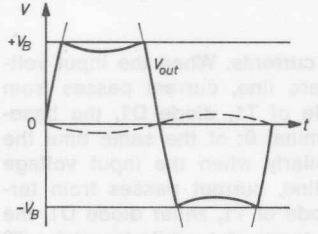


c)

5. RMS Stabilizer for AC
   a) Circuit diagram
   b) Output waveform a low input voltages
   c) Output waveform at high input voltages

High-Symmetry AC Stabilizer

The conventional AC clipper circuit incorporating back-to-back zener diodes has the disadvantage that in order to obtain a good symmetry, the diodes must be quite closely matched. Such diodes are, however, virtually unobtainable in large quantities. Nevertheless a square or trapezoidal waveform of good symmetry is often required for calibration purposes (in oscilloscopes, for example).

In the circuit shown in Fig. 6a the problem has been solved by shunting a zener diode across the DC terminals of a bridge rectifier. When the input goes positive with respect to the zero line, current passes from terminal 1, via series resistor *R* and the diodes D2, D1, and D5, to the zero line, and when it goes negative it passes from terminal 0, via diodes D3, D1, D4, and resistor *R*, back to terminal 1; diode D1 consequently always carries a reverse current. This has the effect of clipping both the positive and negative half waves of the input V_{in} to a level which depends on the forward voltages of the two conventional diodes and the operating voltage of the zener diode, i. e.

$$+ V_{out} = V_{FD2} + V_Z + V_{FD5}$$

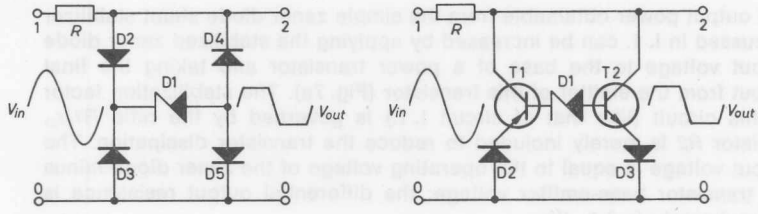
and

$$- V_{out} = V_{FD3} + V_Z + V_{FD4}.$$

By choice of a correct operating point and operating voltage for the zener diode it is possible to attain a certain degree of temperature compensation of the output.

Fig. 6b shows a clipper circuit for higher currents. When the input voltage goes positive with respect to the zero line, current passes from terminal 1, via *R*, the collector-base diode of T1, diode D1, the base-emitter diode of T2 and diode D3, to terminal 0; at the same time the base current turns on transistor T2. Similarly when the input voltage goes negative with respect to the zero line, current passes from terminal 0, via diode D2, the base-emitter diode of T1, zener diode D1, the base-collector diode of T2, and *R*, back to terminal 1, while transistor T2 is now turned on.

As can be seen, the zener diode need only pass the base current of either T1 or T2, which is considerably lower than the associated collector current, I_B being equal to I_C/h_{FE}, where h_{FE} is the DC current gain. In this way it is possible to use high-power transistors capable of passing a high shunt current and yet employ a low-power zener diode. Diodes D2 and D3 must be able to carry the full shunt current but are only necessary when the operating voltage of zener diode D1 exceeds the maximum permissible transistor emitter-base voltage V_{EB0} (approximately 5 . . . 7 V for diffused silicon transistors).



6. High-symmetry AC stabilizer
   a) Low-current circuit
   b) Heavy-current circuit

Simple Series Stabilizers

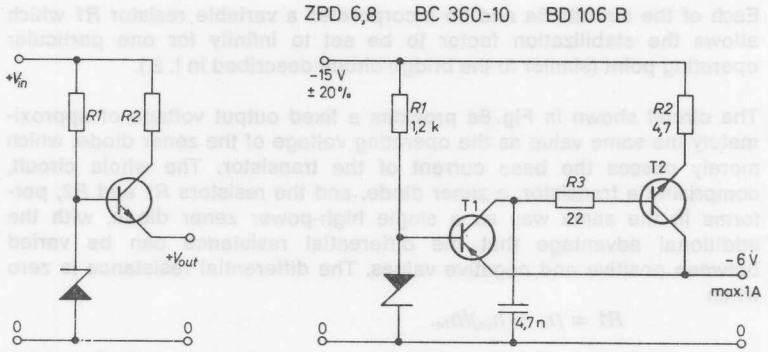
The output power obtainable from the simple zener diode shunt stabilizer discussed in I. 1. can be increased by applying the stabilized zener diode output voltage to the base of a power transistor and taking the final output from the emitter of this transistor (Fig. 7a). The stabilization factor of this circuit (like that of circuit I. 1.) is governed by the ratio $R1/r_z$. Resistor *R2* is merely included to reduce the transistor dissipation. The output voltage is equal to the operating voltage of the zener diode minus the transistor base-emitter voltage; the differential output resistance is approximately $(r_z + h_{ie})/h_{FE}$.

A further reduction in output resistance can be obtained by employing a so-called Lin-circuit, of which the circuit shown in Fig. 7b is a design example. Here a PNP transistor T1 and an NPN transistor T2 are connected in such a way that the circuit performs very much like a single transistor stage with a current gain of $h_{FE\,1} \cdot h_{FE\,2}$, which, however, has an input impedance h_{ie} equal to that of T1 only. Connecting the transistors in this way reduces the output resistance of the stage well below that of circuit 7a. The resistor *R3* is added to provide overload protection for T1; the capacitor prevents unwanted oscillation. The measured mean output resistance was found to be as follows:

2 Ω in the range $I_L =$ 0 . . . 50 mA,
0.1 Ω in the range $I_L =$ 50 . . . 500 mA,
0.02 Ω in the range $I_L =$ 0.5 . . . 1 A

As can be seen, the output resistance is current-dependent. At $I_L =$ 500 mA the stabilization factor S is > 50.

The power transistor must be mounted on a heat sink with a thermal resistance not exceeding 15 °C/W. In supplies designed to give a positive output with respect to chassis, the transistor case (which is directly connected to the collector) need not be insulated from the chassis. If the load current is less than 0.6 A, then the circuit can be short-circuit protected simply by increasing the value of *R2* to 8.2 Ω, in which case *R2* must be capable of dissipating 40 W under short-circuit conditions.



7. Simple series stabilizers
   a) Incorporating series transistor
   b) Incorporating two-transistor Lin-circuit

Simple Shunt Stabilizers

Each of the circuits 8a and 8b incorporates a variable resistor *R1* which allows the stabilization factor to be set to infinity for one particular operating point (similar to the bridge circuit described in I. 2.).

The circuit shown in Fig. 8a provides a fixed output voltage of approximately the same value as the operating voltage of the zener diode, which merely passes the base current of the transistor. The whole circuit, comprising a transistor, a zener diode, and the resistors *R1* and *R2*, performs in the same way as a single high-power zener diode, with the additional advantage that the differential resistance can be varied between positive and negative values. The differential resistance is zero when

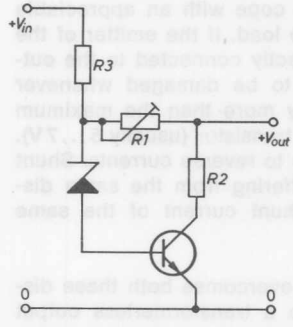
$$R1 = (r_z + h_{ie})/h_{fe}.$$

If the input voltage is increased, then the current through the zener diode and hence the base and collector current of the transistor increase also. This causes the voltage dropped across *R3* and preset control *R1* to increase, with the result that the original rise in input voltage is compensated for and V_{out} is kept constant.

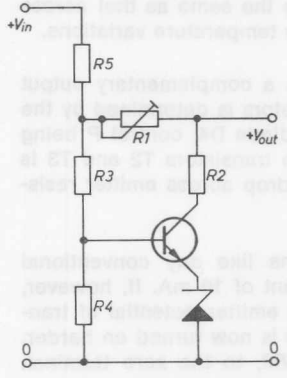
Circuit 8b is an improvement on circuit 8a in that it permits the output to be adjusted by variation of the *R3/R4* ratio; it has the disadvantage that the zener diode must be capable of carrying the full emitter current of the transistor. The balance equation for this circuit is

$$R1 = (r_z + h_{ie}/h_{fe}) \cdot (R3 + R4)/R4.$$

At balance the output resistance of either circuit is approximately equal to *R1*.



8 a. Shunt stabilizer for fixed output voltage



8 b. Shunt stabilizer giving variable output voltage

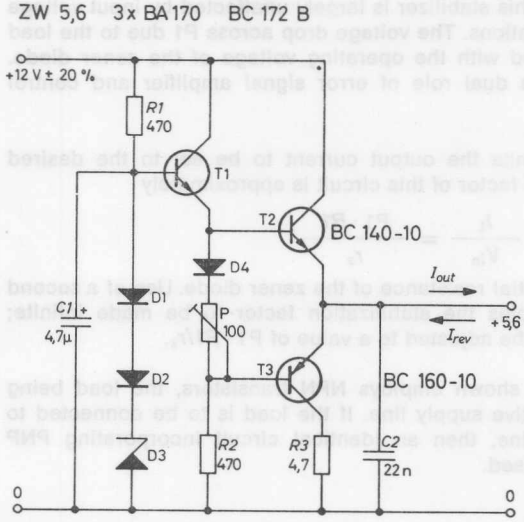
Combined Series-Shunt Stabilizer

Conventional series stabilizers are unable to cope with an appreciable back-EMF or reverse current produced by the load. If the emitter of the series transistors used in the stabilizer is directly connected to the output (see I. 7.), then this transistor is likely to be damaged whenever the back EMF exceeds the output voltage by more than the maximum permissible emitter-base voltage of the series transistor (usually 5...7 V). Such a supply presents a very high resistance to reverse currents. Shunt stabilizers, on the other hand, whilst not suffering from the same disadvantages, pass a continuous quiescent shunt current of the same order of magnitude as the output current.

The combined circuit shown in Fig. 9 largely overcomes both these disadvantages. In principle it is very similar to a transformerless output stage familiar from audio engineering, and consists, in the main, of a Darlington pair formed by transistors T1 and T2. A stabilized voltage derived from zener diode D3 is applied to the base of T1. Two diodes, D1 and D2, are connected in series with D3 to compensate for any loss in voltage caused by the base-emitter threshold voltages of T1 and T2. The output voltage V_{out} is consequently largely the same as that across zener diode D3 and is reasonably unaffected by temperature variations.

NPN transistor T2 and PNP transistor T3 form a complementary output stage. The operating point of both these transistors is determined by the voltage dropped across preset control P and diode D4, control P being adjusted so that the quiescent current through transistors T2 and T3 is approximately 10 mA, i. e. so that the voltage drop across emitter resistor *R3* is approximately 50 mV.

Under normal conditions the circuit functions like any conventional series regulator, and passes a quiescent current of 10 mA. If, however, a back EMF is applied to the output, then the emitter potential of transistor T3 becomes more positive. Transistor T3 is now turned on harder, and the reverse current passes, via T3 and *R3,* to the zero terminal. Capacitor *C1* provides additional filtering for the reference voltage, whilst *C2* prevents instability. Each of the output transistors T2 and T3 should be fitted with a heat dissipator, p. ex. KS 1.



9. Combined series-shunt stabilizer

Performance Specifications

Input voltage	$V_{in} = 12\ V \pm 20\ \%$
Output voltage	$V_{out} \approx 5.6\ V\ (V_{out} \approx V_Z)$
Max. load current	$I_{out} = 200\ mA$
Stabilization factor	$S > 50$
Output resistance	$r_{out} \approx 20\ m\Omega$
Max. reverse current	$I_{rev} = 200\ mA$
Output reverse resistance	$r_{rev} \approx 1\ \Omega$
Required thermal resistance of the sink	$R_{th\,S} < 50\ °C/W$

Simple Current Stabilizer (Constant Current Source)

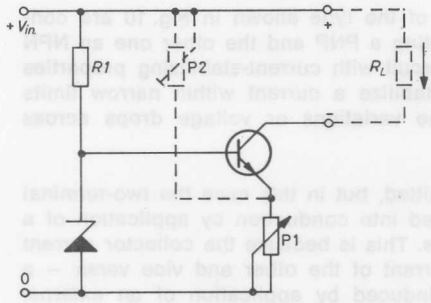
The output current of this stabilizer is largely unaffected by input voltage or load resistance variations. The voltage drop across P1 due to the load current, I_L, is compared with the operating voltage of the zener diode. The transistor has the dual role of error signal amplifier and control element.

Potentiometer P1 permits the output current to be set to the desired value. The stabilization factor of this circuit is approximately

$$S_I = \frac{dV_{in}}{dI_L} \cdot \frac{I_L}{V_{in}} = \frac{P1 \cdot R1}{r_z}$$

where r_z is the differential resistance of the zener diode. Use of a second potentiometer P2 enables the stabilization factor to be made infinite; P2 would then have to be adjusted to a value of $P1 \cdot R1/r_z$.

The current stabilizer shown employs NPN transistors, the load being connected to the positive supply line. If the load is to be connected to the negative supply line, then an identical circuit incorporating PNP transistors should be used.



10. Simple current stabilizer (constant current source)

Two-Terminal Constant Current Circuit

If two constant current sources of the type shown in Fig. 10 are connected in parallel, one incorporating a PNP and the other one an NPN transistor, then a two-terminal circuit with current-stabilizing properties is formed. Such a circuit will stabilize a current within narrow limits irrespective of any input voltage variations or voltage drops across other loads.

Resistors P and *R2* could be omitted, but in this case the two-terminal device would have to be triggered into conduction by application of a current pulse to one of the bases. This is because the collector current of one transistor is the base current of the other and vice versa – a state which must be artifically induced by application of an external signal. The presence of resistor *R2* (approx. 1 MΩ) ensures that this happens automatically.

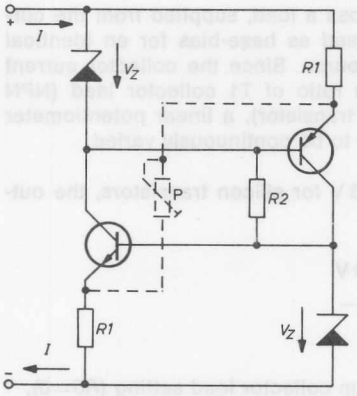
Whether *R2* is used or not, the preset control P is important; without it an increase in terminal voltage would result in a slight current rise, which this control allows to be compensated for.

If P is reduced below the optimum value giving maximum current stabilization, then the two-terminal device exhibits a resistance characteristic which, under certain conditions, is negative.

The voltage dropped across either of the two resistors *R1,* and hence the current through them is virtually constant, the voltage being approximately equal to V_Z. The collector current of both transistors is equal to this constant current minus the current passing through variable resistor P (base-currents are disregarded). Whilst any voltage increase across the two-terminal network causes the current through this resistor to increase, this is offset by an equal reduction of the current through the two transistors; therefore the total current through the two-terminal device falls by the same amount as that by which the current through P is increased. The two-terminal device consequently has a negative differential resistance of -P, provided the resistance of *R2* is very much higher than that of P.

The usable negative resistance range is limited by the terminal voltages $2\ V_Z$ and $(P/R1 + 2) \cdot V_Z$. If the terminal voltage is too low, then the diodes carry hardly any current, and if it is too high, then the transistors are cut off.

This easily adjustable device, because of its ability to maintain a constant negative resistance over a wide range of operating conditions, could be used, for example, to nullify the effect of a positive resistance in a circuit in which a constant current is to be maintained.



11. Two-terminal constant current circuit

Wide Range Constant Current Source

In this circuit the voltage dropped across a load, supplied from the current stabilizer discussed in I. 10., is used as base-bias for an identical but complementary constant current source. Since the collector current of transistor T2 is proportional to the ratio of T1 collector load (NPN transistor) to T2 emitter resistor (PNP transistor), a linear potentiometer is incorporated which permits this ratio to be continuously varied.

Assuming a base emitter voltage of 0.6 V for silicon transistors, the output current works out to

$$I_L = \frac{\frac{V_Z - 0.6\ V}{R4} \cdot (R2 + R5) - 0.6\ V}{R3 + R6}$$

and is

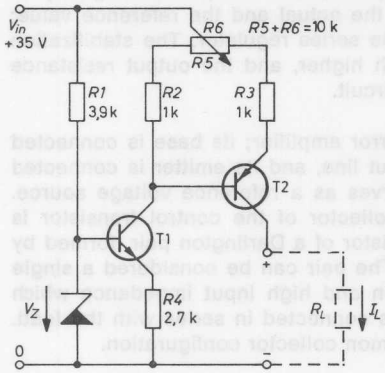
approximately 0.15 mA for the minimum collector load setting ($R5 = 0$),
approximately 2.2 mA with the wiper in the centre ($R5 = R6$), and
approximately 24.5 mA for the minimum emitter resistance setting ($R6 = 0$)
of the potentiometer.

The variation range is consequently 24.5 : 0.15 = 163 : 1. The reduction in output current due to the finite current gain of transistors T1 and T2 is negligible. The circuit is designed to give an output voltage of between 0 and 5 V.

When the circuit is to be designed for different output currents and voltages, is should be borne in mind that the voltage difference $V_{in} - V_Z$ must exceed the maximum possible voltage drop across $R2 + R5$. This voltage drop also sets a limit to the maximum possible voltage that can be developed across the load R_L. If very low currents are to be stabilized and the circuit is consequently designed as a high-impedance device, then the load current should not be reduced to below 1 µA as otherwise difficulties due to the leakage current of transistor T2 may be experienced.

The circuit could have applications in wide range timers and function generators, to provide a constant charging current for the timing capacitor (in a Miller integrator, for example). The device replaces in this case the conventional charge or discharge resistor but has the advantage that the value of any capacitors used in long time constant circuits can be drastically reduced.

ZPD 6,8 BC 171 B BC 251 B



12. Wide range constant current source

Series Stabilizer

This circuit, unlike that of the very simple series stabilizer discussed in I. 7., incorporates an error signal amplifier, which amplifies a signal proportional to the difference between the actual and the reference value; the amplified signal then controls the series regulator. The stabilization factor attainable in this way is much higher, and the output resistance much lower than that of the simple circuit.

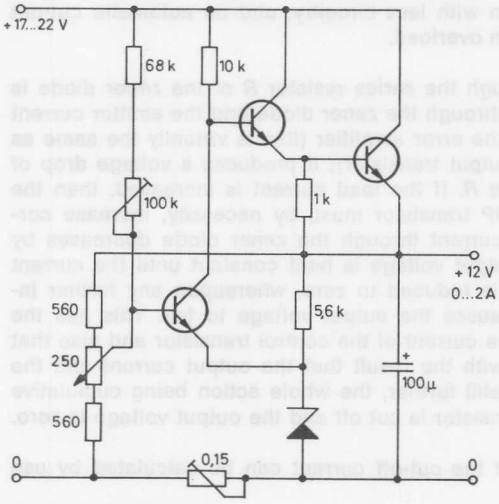
Transistor BC 170 functions as an error amplifier; its base is connected to a voltage divider across the output line, and its emitter is connected to a zener diode ZPD 6.2 which serves as a reference voltage source. The amplified error signal at the collector of the control transistor is applied to the base of the first transistor of a Darlington pair, formed by transistors BC 140-6 and 2 N 3055. The pair can be considered a single series transistor of high current gain and high input impedance which forms part of the main circuit, i. e. is connected in series with the load. The Darlington pair functions in common collector configuration.

If the output voltage rises, then the base of control transistor BC 170 becomes more positive. This causes the collector current and hence the voltage dropped across the 10 kΩ collector load to increase, with the result that the BC 140-6 base voltage and hence the output voltage is reduced, and the original voltage rise is largely corrected.

The residual output variations of such a proportional control system, whether these are due to input voltage or load current variations, can be eliminated by feedforward of the disturbance variable, the 100 kΩ potentiometer being provided for this purpose. This should be adjusted so that the output voltage is not affected by any input voltage changes. Stabilization factors of approximately 100 can be attained in this way. The 250 Ω potentiometer is an incremental output control; the variable 150 mΩ resistor permits the output resistance of the stabilizer to be reduced to zero.

The 2 N 3055 transistor must be mounted on a heat sink with a thermal resistance not exceeding 5 °C/W; the BC 140 should be fitted with a push-on heat dissipator (e. g. KS 1). The circuit may then be operated at ambient temperatures up to +45 °C. Note that the output must not be short-circuited.

BC 170 B BC 140-6 ZPD 6,2 2N 3055



13. Series stabilizer

Short-Circuit Protected Complementary Transistor Series Stabilizer

Use of two complementary transistors permits the principle on which circuit I. 13. is based to be modified so as to gain two advantages, namely better stabilization with less circuitry, and an automatic cut-out action on application of an overload.

The current passing through the series resistor R of the zener diode is composed of the current through the zener diode and the emitter current of the transistor forming the error amplifier (this is virtually the same as the base current of the output transistor); it produces a voltage drop of approximately 17 V across R. If the load current is increased, then the emitter current of the PNP transistor must, by necessity, increase correspondingly, whilst the current through the zener diode decreases by the same amount. The output voltage is held constant until the current through the zener diode is reduced to zero, whereupon any further increase in load current causes the output voltage to fall. This has the effect of reducing the base current of the control transistor and also that of the output transistor, with the result that the output current and the output voltage decrease still further, the whole action being cumulative until finally the output transistor is cut off and the output voltage is zero.

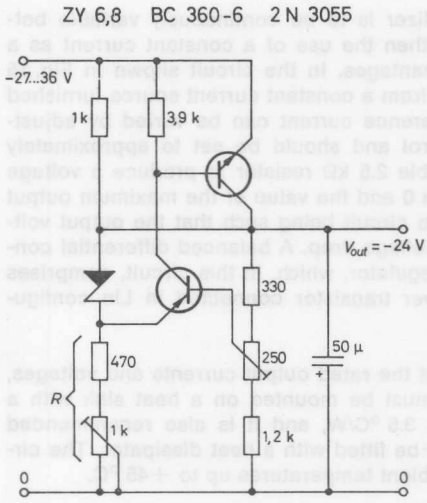
The approximate value of the cut-off current can be calculated by use of the formula

$$I_{max} = (V_{out} - V_Z)h_{FE}/R$$

where h_{FE} is the current gain of the output transistor (taking into account the current passing through the 3.9 kΩ base-emitter resistor) and V_Z is the operating voltage of the zener diode.

Because of the 1 kΩ resistor the circuit still produces a small quiescent output voltage decrease still further, the whole action being cumulative necessary to permit the circuit to reset itself to normal after the short circuit or the cause of the overload has been removed. To achieve this the load must be reduced until the voltage drop across it due to the quiescent current exceeds the base-emitter turn-on voltage of the PNP transistor.

The 250 Ω preset control permits the output voltage to be set to the exact required value. The 1 kΩ potentiometer is a cut-out current control which permits several stabilizers to be set so that they cut out at the same current regardless of the spread in current gain of the output transistors.



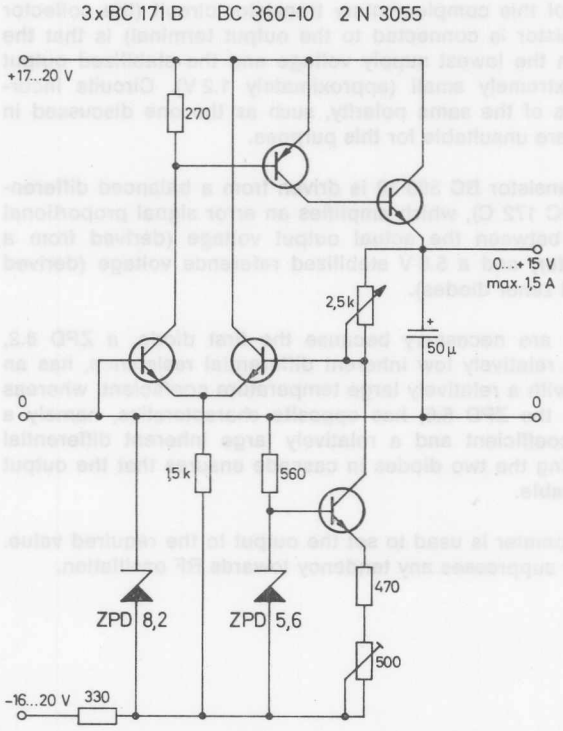
14. Short-circuit protected complementary transistor series stabilizer

Series Stabilizer with Variable Output Voltage

If the output voltage of a stabilizer is to be continuously variable between 0 and a maximum value, then the use of a constant current as a reference value has certain advantages. In the circuit shown in Fig. 15 the reference current is derived from a constant current source furnished by an ancillary supply. The reference current can be varied by adjustment of the 500 Ω preset control and should be set to approximately 7 mA. It passes through a variable 2.5 kΩ resistor to produce a voltage drop that can be varied between 0 and the value of the maximum output voltage, the control action of the circuit being such that the output voltage is always the same as this voltage drop. A balanced differential control amplifier drives the series regulator, which, in this circuit, comprises a PNP driver and an NPN power transistor connected in Lin configuration.

To remove the heat generated at the rated output currents and voltages, the 2 N 3055 power transistor must be mounted on a heat sink with a thermal resistance of less than 3.5 °C/W, and it is also recommended that the driver transistor BC 360 be fitted with a heat dissipator. The circuit can then be operated at ambient temperatures up to +45 °C.

The circuit has a stabilization factor of approximately 100 and an output resistance of approximately 30 . . . 40 mΩ.



15. Series stabilizer with variable output voltage

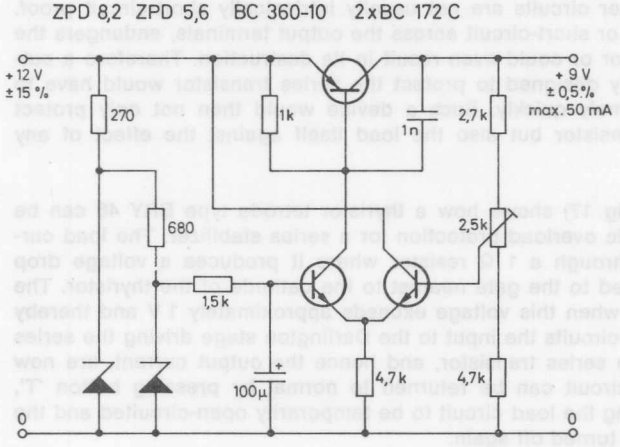
Series Stabilizer with Low Voltage Drop

The main feature of this complementary transistor circuit (the collector of the series transistor is connected to the output terminal) is that the difference between the lowest supply voltage and the stabilized output voltage can be extremely small (approximately 1.2 V). Circuits incorporating transistors of the same polarity, such as the one discussed in I. 13. for example, are unsuitable for this purpose.

The PNP series transistor BC 360-10 is driven from a balanced differential amplifier (2 x BC 172 C), which amplifies an error signal proportional to the difference between the actual output voltage (derived from a 2.5 kΩ potentiometer) and a 5.6 V stabilized reference voltage (derived from two cascaded zener diodes).

Two zener diodes are necessary because the first diode, a ZPD 8.2, whilst exhibiting a relatively low inherent differential resistance, has an operating voltage with a relatively large temperature coefficient, whereas the second diode, the ZPD 5.6, has opposite characterstics, namely a low temperature coefficient and a relatively large inherent differential resistance. Operating the two diodes in cascade ensures that the output voltage is highly stable.

The 2.5 kΩ potentiometer is used to set the output to the required value. The 1 nF capacitor suppresses any tendency towards RF oscillation.



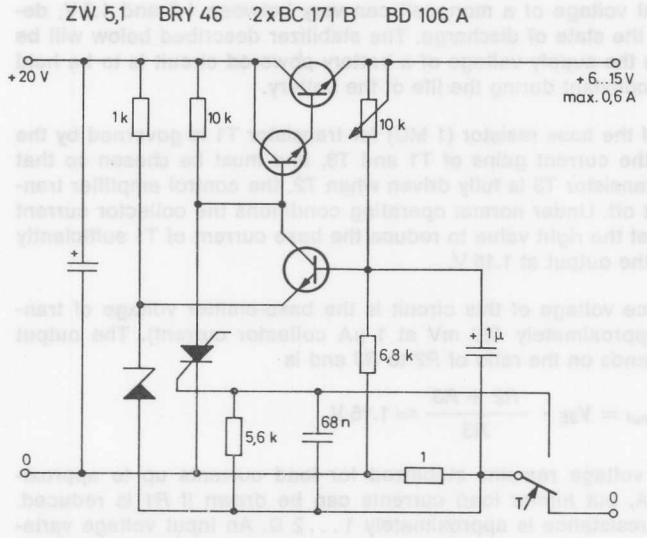
16. Series stabilizer with low voltage drop

Series Stabilizer with Electronic Cut-Out

Series stabilizer circuits are not usually intrinsically short-circuit proof. Any overload, or short-circuit across the output terminals, endangers the series transistor or could even result in its destruction. Therefore a cut-out specifically designed to protect the series transistor would have to operate extremely quickly. Such a device would then not only protect the series transistor but also the load itself against the effect of any overload.

The circuit (Fig. 17) shows how a thyristor tetrode type BRY 46 can be used to provide overload protection for a series stabilizer. The load current passes through a 1 Ω resistor where it produces a voltage drop which is applied to the gate nearest to the cathode of the thyristor. The thyristor fires when this voltage exceeds approximately 1 V and thereby virtually short-circuits the input to the Darlington stage driving the series transistor. The series transistor, and hence the output current, are now cut off. The circuit can be returned to normal by pressing button 'T', thereby causing the load circuit to be temporarily open-circuited and the thyristor to be turned off again.

The 10 kΩ potentiometer permits the output voltage to be continuously varied between 6 and 15 V. The 1 Ω resistor, as well as providing the thyristor with a trigger signal, also introduces a feedforward signal proportional to the disturbance variable (refer to circuit I. 13.), an arrangement which considerably reduces the output resistance of the stabilizer.



17. Series stabilizer with electronic cut-out

Stabilizer for Low Battery Voltages

The terminal voltage of a monocell can vary between 1.7 and 1.2 V, depending on the state of discharge. The stabilizer described below will be of use when the supply voltage of a battery-powered circuit is to be held reasonably constant during the life of the battery.

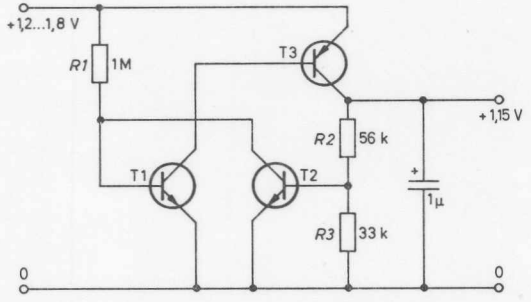
The value of the base resistor (1 MΩ) for transistor T1 is governed by the product of the current gains of T1 and T3, and must be chosen so that the series transistor T3 is fully driven when T2, the control amplifier transistor, is cut off. Under normal operating conditions the collector current of T2 has just the right value to reduce the base current of T1 sufficiently to stabilize the output at 1.15 V.

The reference voltage of this circuit is the base-emitter voltage of transistor T2 (approximately 420 mV at 1 μA collector current). The output voltage depends on the ratio of *R2* to *R3* and is

$$V_{out} = V_{BE} \cdot \frac{R2 + R3}{R3} \approx 1.15\ \text{V}.$$

The output voltage remains stabilized for load currents up to approximately 5 mA, but higher load currents can be drawn if *R1* is reduced. The output resistance is approximately 1 . . . 2 Ω. An input voltage variation from 1.2 to 1.8 V causes the output voltage to vary by not more than approximately 70 mV.

2 x BC 172 C BC 252 C



18. Stabilizer for low battery voltages

II. Amplifiers

Contents

General-Purpose AF Amplifier

The circuit shown in Fig. II. 1. is that of a general-purpose two-stage AF amplifier which is directly coupled, to save components. Use of two DC negative feedback loops – one from the emitter of the second transistor to the base of the first, and the other one from the collector of the second transistor to the emitter of the first – stabilizes the operating point of the amplifier to such an extent that it is largely independent of voltage and temperature changes as well as transistor parameter spreads.

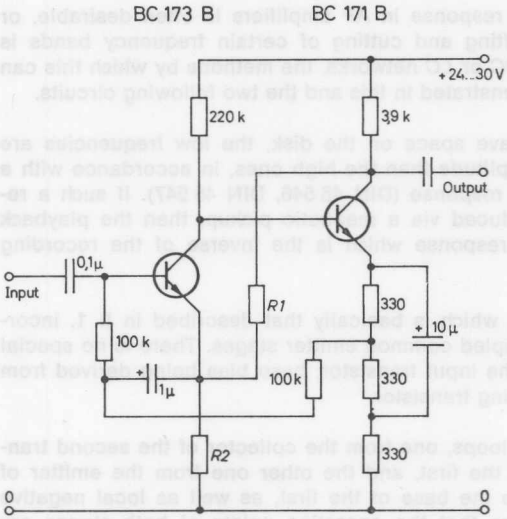
The voltage gain of the amplifier depends almost entirely on the attenuation of the negative feedback voltage divider interposed between the collector of the second transistor and the emitter of the first, and is, therefore, also very stable and quite unaffected by the factors mentioned above. The table below lists various gain and input impedance figures and the associated component values.

Voltage Gain Factor	Voltage Gain in dB	R1 kΩ	R2 kΩ	Input Impedance MΩ
10	20	39	3.9	2
20	26	47	2.2	1
50	34	100	1.8	0.35
100	40	100	0.91	0.2

Practically any frequency response can be attained if the resistive feedback network is replaced by a reactive one, such as an *RC* network. This principle is used, for example, in the recording response equalizer described further on. Another feature of this amplifier is that any unwanted open loop gain is reduced by application of negative feedback, with a consequent reduction in distortion.

The amplifier described will perform just as well with NPN transistors, such as the types BC 253 and BC 251, but in this case the polarity of the supply and that of the electrolytics must be reversed.

The current consumption of the amplifier is approximately 3 mA, and the output impedance is approximately 1 kΩ. The value of the output coupling capacitor depends on the input impedance and LF response requirements of the following amplifier.



1. General-purpose AF amplifier

Recording Response Equalizer with Rumble and Noise Filter

A non-linear frequency response in AF amplifiers is often desirable, or even necessary. The lifting and cutting of certain frequency bands is effected by the use or *RC* or *LC* networks, the methods by which this can be achieved being demonstrated in this and the two following circuits.

In disk recording, to save space on the disk, the low frequencies are recorded at a lower amplitude than the high ones, in accordance with a standardized recording response (DIN 45 546, DIN 45 547). If such a recording is to be reproduced via a magnetic pickup, then the playback amplifier must have a response which is the inverse of the recording response.

The equalizer/amplifier, which is basically that described in II. 1. incorporates two directly coupled common emitter stages. There is no special base bias network for the input transistor, base bias being derived from the emitter of the following transistor.

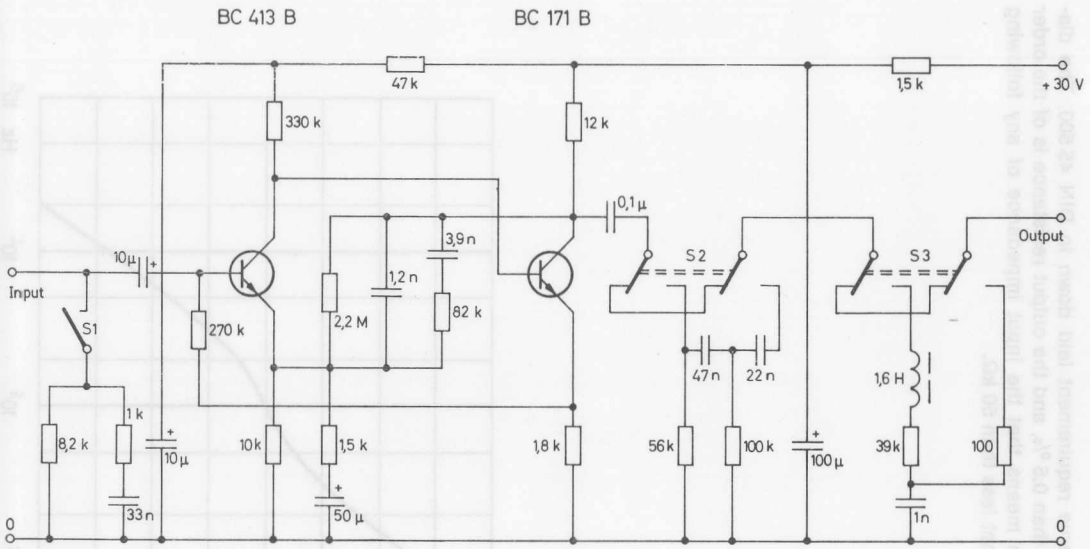
Two negative feedback loops, one from the collector of the second transistor to the emitter of the first, and the other one from the emitter of the second transistor to the base of the first, as well as local negative current feedback, ensure that the operating points of both stages are well stabilized. The design of the network is such that more feedback is applied at the higher than at the lower frequencies, thus providing the required bass lift.

Magnetic pickups produce a velocity-proportional EMF (deflection velocity of the needle), while crystal pickups produce an amplitude-proportional EMF. The equalizer/amplifier, which, in the described form, is suitable for the connection of a magnetic pickup, can be modified for use with a crystal pickup simply by providing a switch S1 which connects an *RC* network across the input.

Another switch S2 brings into circuit a rumble filter which attenuates all frequencies below 30 Hz and is an example of how the frequency response of an amplifier can be modified by use of an *RC* highpass filter.

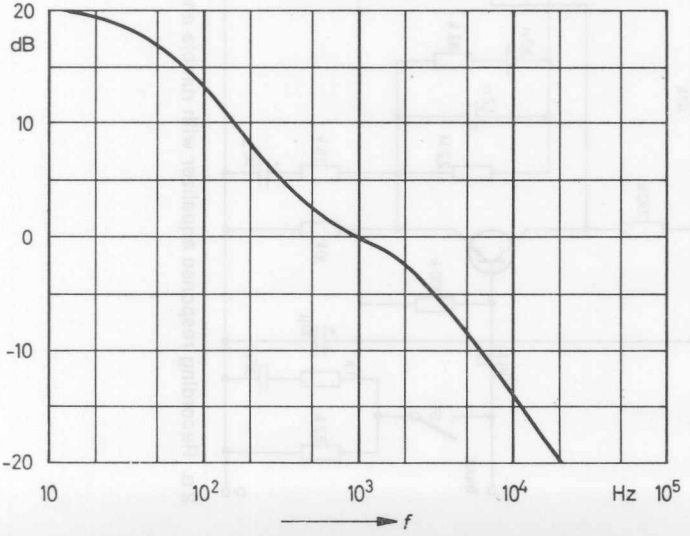
Switch S3 connects into circuit an *LC* noise filter, comprising a series-resonant circuit tuned to approximately 4 kHz; this circuit is heavily damped so as to produce only a slight lift in response about the resonant frequency, whilst signals above resonance are rapidly attenuated.

The amplifier, which has a current consumption of approximately 1 mA, provides a gain of approximately 50 (≙ 34 dB) at 1 kHz, so that an input of 10 mV (magnetic pickup) produces an output of 500 mV. However, the amplifier can be driven up to an output level of 4 V to comply with the

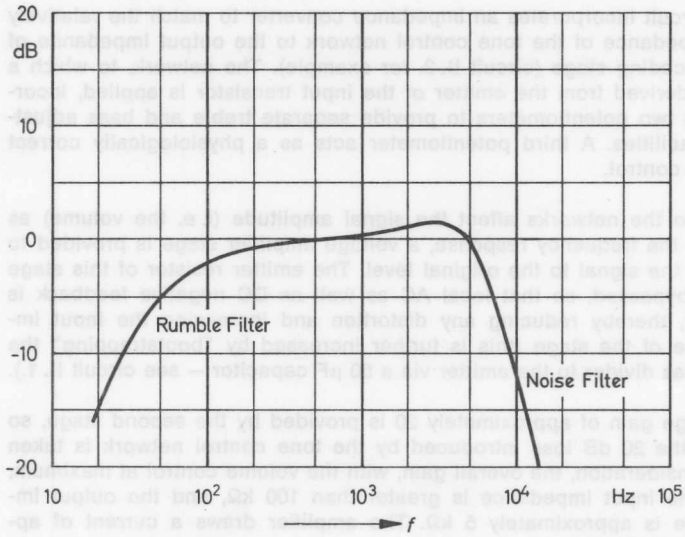


2 a. Recording response equalizer with rumble and noise filter

12 dB overload reserve requirement laid down in DIN 45 500. The distortion factor is less than 0.5 %, and the output resistance is of the order of several kΩ, which means that the input impedance of any following amplifier should be not less than 50 kΩ.



2 b. Equalizer response



2 c. Response of rumble and noise filter without amplifier

II. 3.

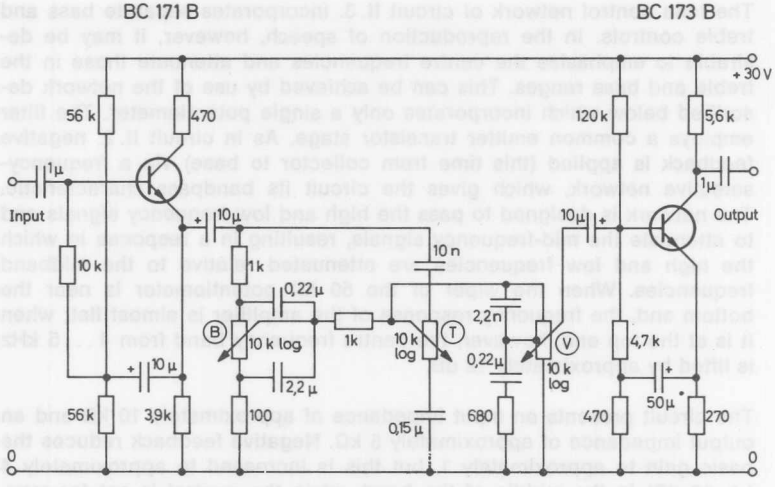
AF Preamplifier with Tone and Volume Controls

This circuit incorporates an impedance converter to match the relatively low impedance of the tone control network to the output impedance of the preceding stage (circuit II. 2. for example). The network, to which a signal derived from the emitter of the input transistor is applied, incorporates two potentiometers to provide separate treble and bass adjustment facilities. A third potentiometer acts as a physiologically correct volume control.

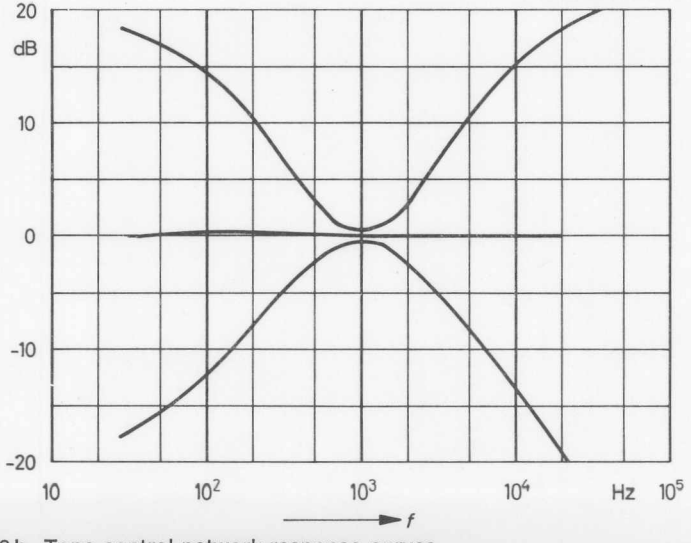
Because the networks affect the signal amplitude (i. e. the volume) as well as the frequency response, a voltage amplifier stage is provided to restore the signal to the original level. The emitter resistor of this stage is not bypassed, so that local AC as well as DC negative feedback is applied, thereby reducing any distortion and increasing the input impedance of the stage (this is further increased by "bootstrapping" the base-bias divider to the emitter via a 50 μF capacitor — see circuit II. 1.).

A voltage gain of approximately 20 is provided by the second stage, so that if the 20 dB loss introduced by the tone control network is taken into consideration, the overall gain, with the volume control at maximum, is 2. The input impedance is greater than 100 kΩ, and the output impedance is approximately 5 kΩ. The amplifier draws a current of approximately 7 mA.

If circuit II. 3. is driven by the output of circuit II. 2. then the input coupling capacitor can be omitted.



3 a. AF Preamplifier with tone and volume controls

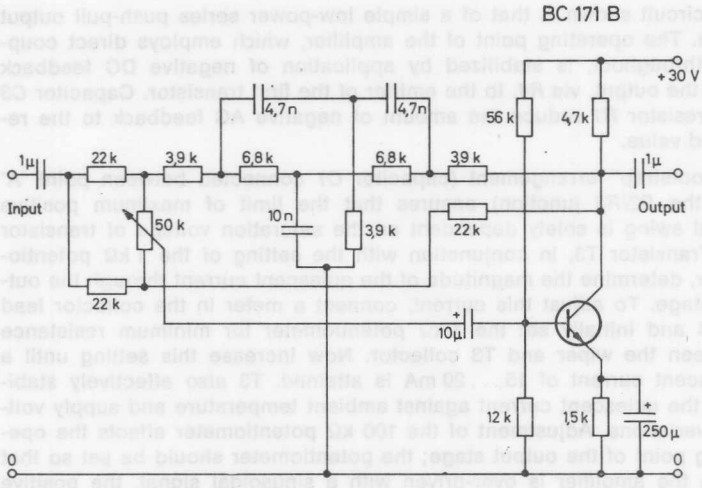


3 b. Tone control network response curves

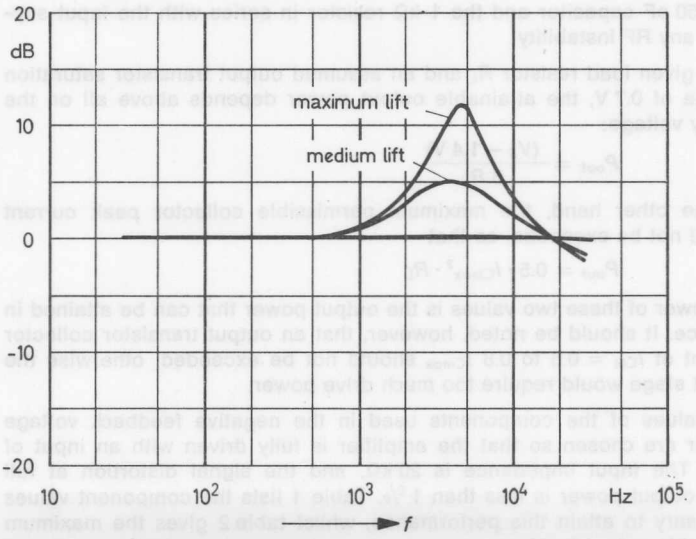
Presence Filter

The tone control network of circuit II. 3. incorporates separate bass and treble controls. In the reproduction of speech, however, it may be desirable to emphasize the centre frequencies and attenuate those in the treble and bass ranges. This can be achieved by use of the network described below which incorporates only a single potentiometer. The filter employs a common emitter transistor stage. As in circuit II. 2. negative feedback is applied (this time from collector to base) via a frequency-selective network, which gives the circuit its bandpass characteristic. The network is designed to pass the high and low-frequency signals and to attenuate the mid-frequency signals, resulting in a response in which the high and low frequencies are attenuated relative to the midband frequencies. When the wiper of the 50 kΩ potentiometer is near the bottom end, the frequency response of the amplifier is almost flat; when it is at the top end, however, the centre frequency band from 4 . . . 5 kHz is lifted by approximately 12 dB.

The circuit presents an input impedance of approximately 10 kΩ and an output impedance of approximately 5 kΩ. Negative feedback reduces the basic gain to approximately 1, but this is increased to approximately 4 (≙ 12 dB) in the middle of the band, when the control is set for maximum lift. The circuit has approximately 3 mA current consumption. The coupling capacitor can be omitted when circuit II. 4. is driven by the output of circuit II. 3.



4 a. Presence filter



4 b. Presence filter response

Low-Power Complementary Series Push-Pull Output Stage

The circuit shown is that of a simple low-power series push-pull output stage. The operating point of the amplifier, which employs direct coupling throughout, is stabilized by application of negative DC feedback from the output, via *R4,* to the emitter of the first transistor. Capacitor *C3* and resistor *R1* reduce the amount of negative AC feedback to the required value.

A "bootstrap" arrangement (capacitor *C1* connected between point 'A' and the *R2*/*R3* junction) ensures that the limit of maximum positive signal swing is solely dependent on the saturation voltage of transistor T4. Transistor T3, in conjunction with the setting of the 1 kΩ potentiometer, determine the magnitude of the quiescent current through the output stage. To adjust this current, connect a meter in the collector lead of T4 and initially set the 1 kΩ potentiometer for minimum resistance between the wiper and T3 collector. Now increase this setting until a quiescent current of 15 . . . 20 mA is attained. T3 also effectively stabilizes the quiescent current against ambient temperature and supply voltage variations. Adjustment of the 100 kΩ potentiometer affects the operating point of the output stage; the potentiometer should be set so that when the amplifier is over-driven with a sinusoidal signal, the positive and negative signal peaks are clipped by the same amount (this occurs when the DC voltage measured at point 'A' is equal to the supply voltage divided by 2).

The 150 pF capacitor and the 1 kΩ resistor in series with the input suppress any RF instability.

For a given load resistor R_L and an assumed output transistor saturation voltage of 0.7 V, the attainable output power depends above all on the supply voltage:

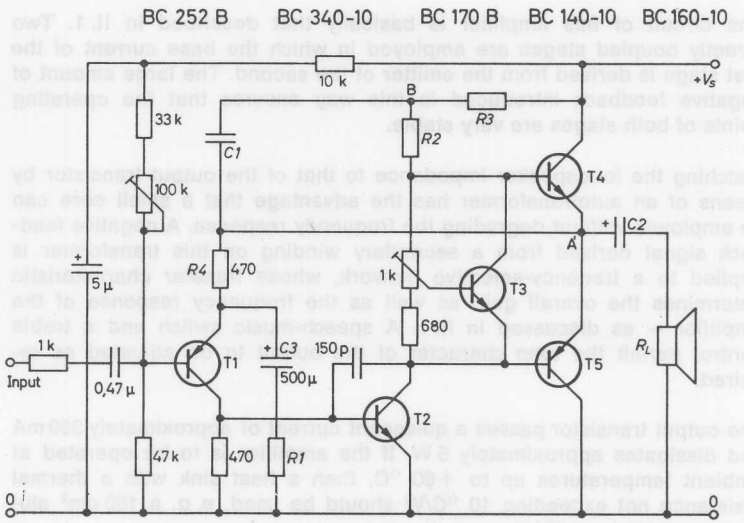
$$P_{out} = \frac{(V_S - 1.4\ \mathrm{V})}{8\ R_L}$$

On the other hand, the maximum permissible collector peak current should not be exceeded, so that

$$P_{out} = 0.5 \cdot I_{Cmax}{}^2 \cdot R_L$$

The lower of these two values is the output power that can be attained in practice. It should be noted, however, that an output transistor collector current of $I_{CM} = 0.6$ to $0.8\ I_{Cmax}$ should not be exceeded, otherwise the output stage would require too much drive power.

The values of the components used in the negative feedback voltage divider are chosen so that the amplifier is fully driven with an input of 0.1 V. The input impedance is 20 kΩ, and the signal distortion at full rated output power is less than 1 %. Table 1 lists the component values necessary to attain this performance, whilst table 2 gives the maximum attainable output levels.



5. Complementary series push-pull output stage

Table 1: Amplifier component values

Component	R_L Ω	$V_S = 6$ V	$V_S = 9$ V	$V_S = 12$ V
R1 Ω	4	27	15	–
	8	27	15	10
	16	–	15	10
R2 = R3 Ω	4	47	47	–
	8	100	100	100
	16	–	220	220
C1 µF	4	100	100	–
	8	50	50	50
	16	–	25	25
C2 µF	4	1000	1000	–
	8	500	500	500
	16	–	–	250

Table 2: Attainable output power P_{out}

R_L Ω	$V_S = 6$ V	$V_s = 9$ V	$V_S = 12$ V
4	0.6 W	1.5 W	–
8	0.36 W	0.95 W	1.7 W
16	–	0.48 W	0.87 W

Single-Ended 1.5 W Class A Amplifier

The circuit of this amplifier is basically that described in II. 1. Two directly coupled stages are employed in which the base current of the first stage is derived from the emitter of the second. The large amount of negative feedback introduced in this way ensures that the operating points of both stages are very stable.

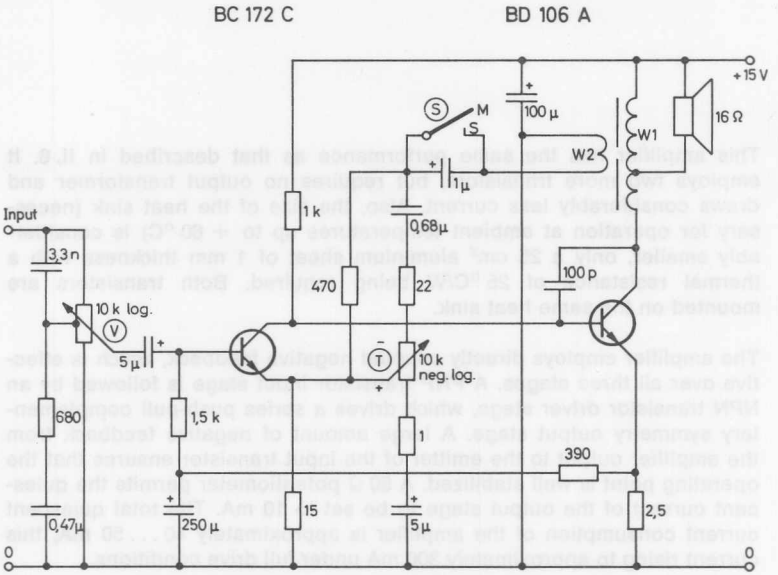
Matching the loudspeaker impedance to that of the output transistor by means of an autotransformer has the advantage that a small core can be employed without degrading the frequency response. A negative feedback signal derived from a secondary winding on this transformer is applied to a freqency-selective network, whose transfer characteristic determines the overall gain as well as the frequency response of the amplifier – as discussed in II. 1. A speech-music switch and a treble control permit the tone character of the output to be adjusted as required.

The output transistor passes a quiescent current of approximately 350 mA and dissipates approximately 5 W. If the amplifier is to be operated at ambient temperatures up to +60 °C, then a heat sink with a thermal resistance not exceeding 10 °C/W should be used, e. g. a 100 cm^2 aluminium sheet 1 mm thick.

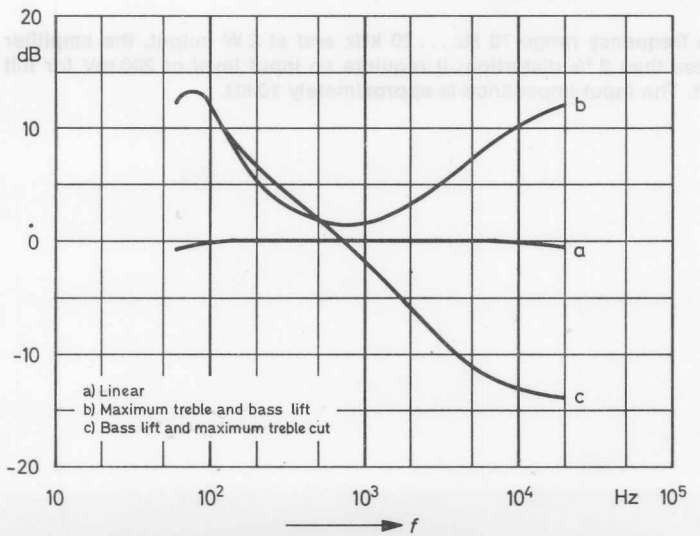
The amplifier has a current consumption of 400 mA; in the 100 Hz . . . 20 kHz frequency range the distortion at 1.5 W output power is less than 3 %. An input of 250 mV is required for full output; the input impedance is approximately 10 kΩ.

Transformer Data

Core: EI 38/14; type IV lamination, 2 x 0.2 mm air gap
Windings: W1 = 230 + 95 turns 0.4 mm dia. en. copper wire
W2 = 325 turns 0.1 mm dia. en. copper wire
Both windings bifilar wound.



6 a. Single-ended 1.5 W class A amplifier



6 b. Amplifier response curves

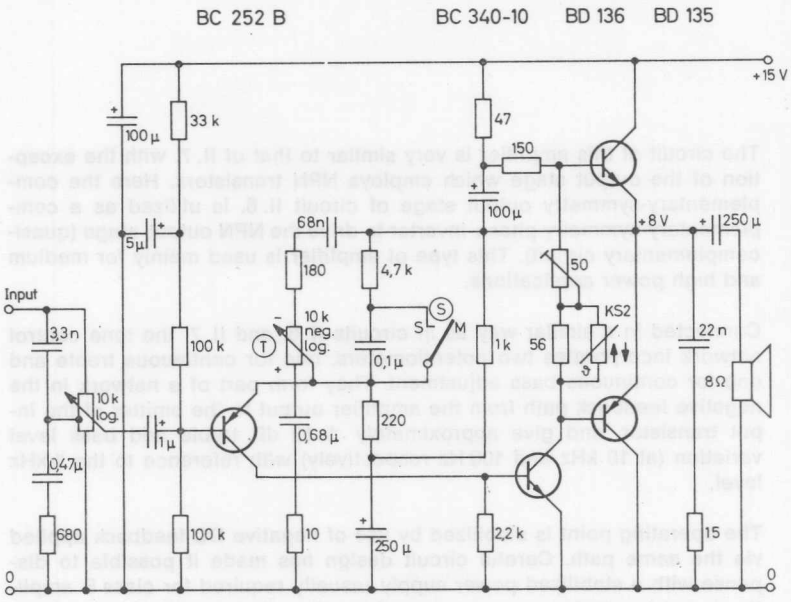
Series Push-Pull 2 W Class B Amplifier

This amplifier has the same performance as that described in II. 6. It employs two more transistors, but requires no output transformer and draws considerably less current. Also, the size of the heat sink (necessary for operation at ambient temperatures up to + 60 °C) is considerably smaller, only a 25 cm^2 aluminium sheet of 1 mm thickness with a thermal resistance of 25 °C/W being required. Both transistors are mounted on the same heat sink.

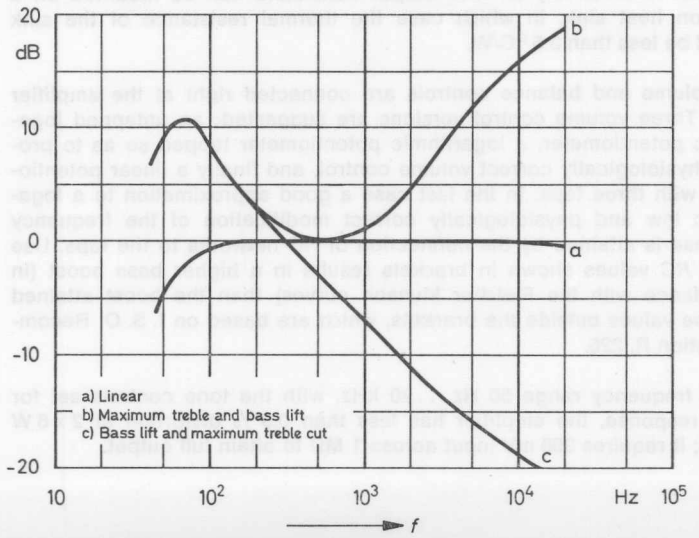
The amplifier employs directly coupled negative feedback, which is effective over all three stages. A PNP transistor input stage is followed by an NPN transistor driver stage, which drives a series push-pull complementary symmetry output stage. A large amount of negative feedback from the amplifier output to the emitter of the input transistor ensures that the operating point is well stabilized. A 50 Ω potentiometer permits the quiescent current of the output stage to be set to 10 mA. The total quiescent current consumption of the amplifier is approximately 40 . . . 50 mA, this current rising to approximately 300 mA under full drive conditions.

As in circuit II. 6. a frequency selective negative feedback network is interposed between the amplifier output and the emitter of the input transistor. Also, as in the previous amplifier, a speech-music switch S and a treble control T are incorporated to permit the tone to be adjusted to individual taste.

In the frequency range 70 Hz . . . 20 kHz and at 2 W output, the amplifier has less than 2 % distortion; it requires an input level of 200 mV for full output. The input impedance is approximately 10 kΩ.



7 a. Series push-pull 2 W class B amplifier



7 b. Amplifier response curves

2 x 6 W Amplifier Conforming to DIN 45 500 (HiFi)

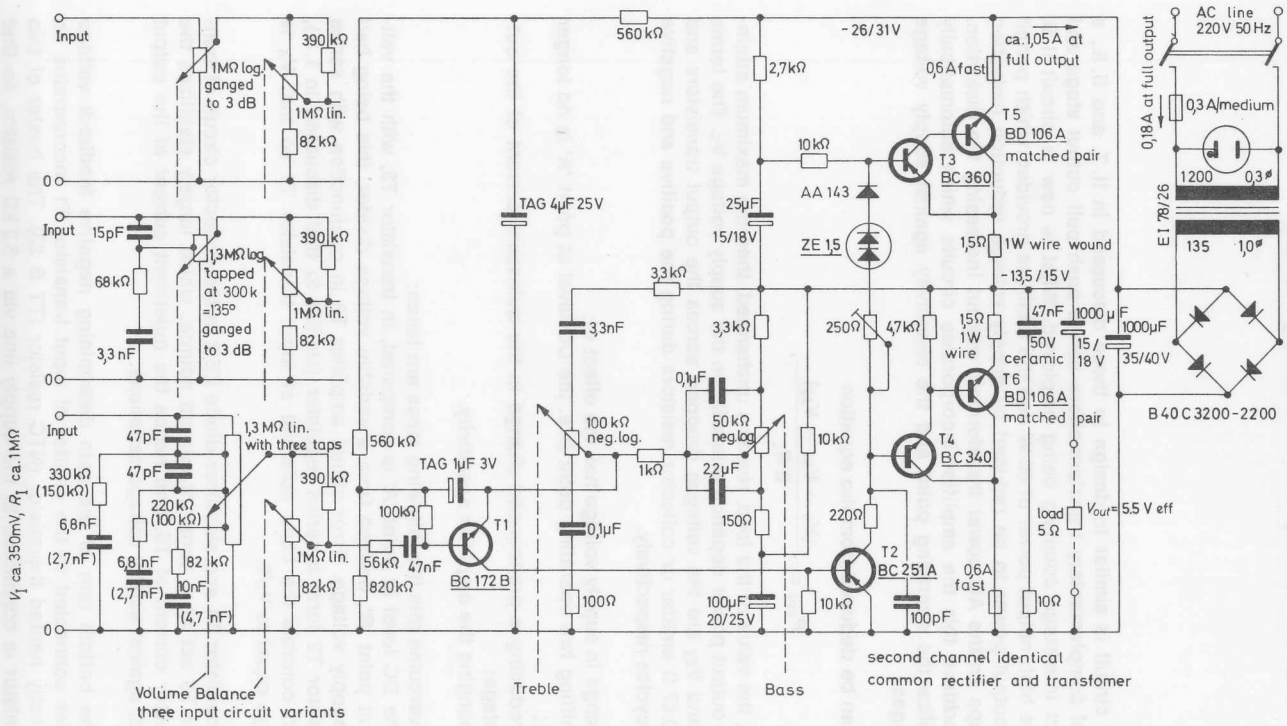
The circuit of this amplifier is very similar to that of II. 7. with the exception of the output stage which employs NPN transistors. Here the complementary-symmetry output stage of circuit II. 6. is utilized as a complementary-symmetry phase inverter to drive the NPN output stage (quasi-complementary circuit). This type of amplifier is used mainly for medium and high power applications.

Connected in a similar way as in circuits II. 6. and II. 7. the tone control network incorporates two potentiometers, one for continuous treble and one for continuous bass adjustment. They form part of a network in the negative feedback path from the amplifier output to the emitter of the input transistor, and give approximately $\pm$ 12 dB treble and bass level variation (at 10 kHz and 100 Hz respectively) with reference to the 1 kHz level.

The operating point is stabilized by use of negative DC feedback applied via the same path. Careful circuit design has made it possible to dispense with a stabilized power supply (usually required for class B amplifiers) and to employ no more smoothing than that provided by a single reservoir capacitor. The quiescent current of the output stage is stabilized against supply and ambient temperature variations by diodes. Each output transistor requires a heat sink with less than 15 °C/W thermal resistance. Alternatively all four output transistors can be mounted on a common heat sink, in which case the thermal resistance of the sink should be less than 3.5 °C/W.

The volume and balance controls are connected right at the amplifier input. Three volume control versions are suggested: an untapped logarithmic potentiometer, a logarithmic potentiometer tapped so as to provide physiologically correct volume control, and finally a linear potentiometer with three taps. In the last case a good approximation to a logarithmic law and physiologically correct modification of the frequency response is attained by the connection of *RC* networks to the taps. Use of the *RC* values shown in brackets results in a higher bass boost (in accordance with the Fletcher Munson curves) than the boost attained with the values outside the brackets, which are based on I. S. O. Recommendation R. 226.

In the frequency range 50 Hz . . . 20 kHz, with the tone controls set for a flat response, the amplifier has less than 0.5 % distortion at 2 x 6 W output; it requires 350 mV input across 1 MΩ to attain full output.



8. 2 x 6 W Amplifier

60 W Amplifier with Output Power Switching Facilities

This circuit is similar in design to those discussed in II. 7. and II. 8., a quasi complementary transformerless series push pull output stage and direct interstage coupling being employed. What is new in circuit II. 9. is the high output power of 60 W and the facilities provided which permit the output power to be reduced by supply voltage reduction (selection of taps on the AC power transformer) without increasing the distortion. To achieve this the amplifier incorporates circuits which automatically stabilize the operating point and the sensitivity against supply voltage changes.

As can be deduced from the equation

$$P_{out} = \frac{(V_S - V_{R1} - V_{R2})}{8\,R_L},$$

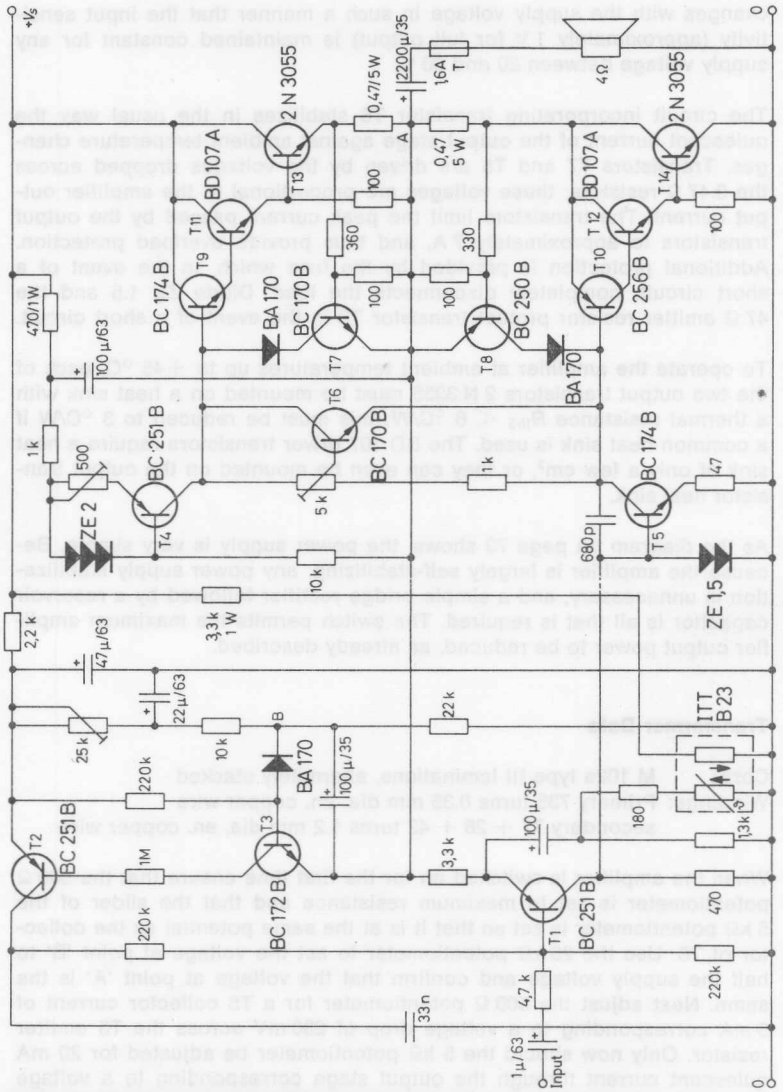
if R_L, the value of the load, remains unchanged, then the maximum attainable output power depends primarily on the supply voltage V_S. The terms V_{R1} and V_{R2} are the voltages dropped across the output transistors and the 0.47 Ω emitter or collector resistors during the positive and negative half-cycles respectively.

A change in supply voltage has the effect of:
1. shifting twe operating point (i. e. the DC level at point 'A' is no longer $V_S/2$);
2. producing a pronounced change in the quiescent current of the output stage;
3. changing the amplifier sensitivity.

To overcome this the following steps are taken:
1. The DC level at point 'A' is compared, in transistor T3, with the voltage at point 'B', derived from a variable voltage divider, this being half the supply voltage. Error signal amplifier T3 in conjunction with series transistor T2 form a series regulator (similar to that discussed in I. 3.), which controls the base potential of input transistor T1 so that V_A is always equal to $V_S/2$.

2. Transistor T4 and stabilizer diode ZE 2 in the collector circuit of transistor T5 act as a constant current source, which largely stabilizes the collector current of T5, and hence the quiescent current of the output stage, against supply voltage variations.

3. The bottom arm of the gain determining negative feedback voltage divider connected to the emitter of input transistor T1 incorporates an indirectly heated thermistor (NTC resistor ITT B 23). The heater of this thermistor is connected to the supply line via a 3.3 kΩ resistor, so that the heater current, and consequently the negative feedback divider ratio,



9 a. 60 W amplifier with output power switching facilities

changes with the supply voltage in such a manner that the input sensitivity (approximately 1 V for full output) is maintained constant for any supply voltage between 20 and 60 V.

The circuit incorporating transistor T6 stabilizes in the usual way the quiescent current of the output stage against ambient temperature changes. Transistors T7 and T8 are driven by the voltages dropped across the 0.47 Ω resistors; these voltages are proportional to the amplifier output current. The transistors limit the peak current passed by the output transistors to approximately 7 A, and thus provide overload protection. Additional protection is provided by the fuse which, in the event of a short circuit, completely disconnects the load. Diode ZE 1.5 and the 47 Ω emitter resistor protect transistor T5 in the event of a short circuit.

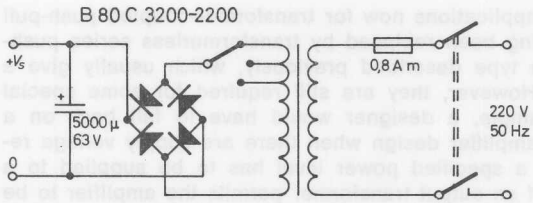
To operate the amplifier at ambient temperatures up to +45 °C, each of the two output transistors 2 N 3055 must be mounted on a heat sink with a thermal resistance $R_{thS} < 6$ °C/W; this must be reduced to 3 °C/W if a common heat sink is used. The BD 107 driver transistors require a heat sink of only a few cm², or they can even be mounted on the output transistor heat sink.

As the diagram on page 73 shows, the power supply is very simple. Because the amplifier is largely self-stabilizing, any power supply stabilization is unnecessary, and a simple bridge rectifier followed by a reservoir capacitor is all that is required. The switch permits the maximum amplifier output power to be reduced, as already described.

Transformer Data

Core: M 102a type III laminations, alternately stacked
Windings: Primary 735 turns 0.35 mm dia. en. copper wire
secondary 77 + 28 + 42 turns 1.2 mm dia. en. copper wire

When the amplifier is switched on for the first time ensure that the 500 Ω potentiometer is set to maximum resistance and that the slider of the 5 kΩ potentiometer is set so that it is at the same potential as the collector of T6. Use the 25 kΩ potentiometer to set the voltage at point 'B' to half the supply voltage and confirm that the voltage at point 'A' is the same. Next adjust the 500 Ω potentiometer for a T5 collector current of 5 mA corresponding to a voltage drop of 230 mV across the T5 emitter resistor. Only now should the 5 kΩ potentiometer be adjusted for 20 mA quiescent current through the output stage corresponding to a voltage drop of approximately 10 mV across one of the 0.47 Ω resistors in this stage. The amplifier is now ready for operation.



9 b. Power supply for 60 W amplifier

Amplifier Data

Output power	at	Supply voltage
15 W		29 V
30 W		40 V
60 W		50 V

Adjustment of the supply voltage between 20 and 60 V permits any output level to be selected.

Frequency response	± 1 dB in the 25 Hz . . . 20 kHz range
Required input for full output	1 V
Distortion at full output	< 0.2 % at 100 Hz < 0.1 % at 1 kHz < 0.25 % at 10 kHz

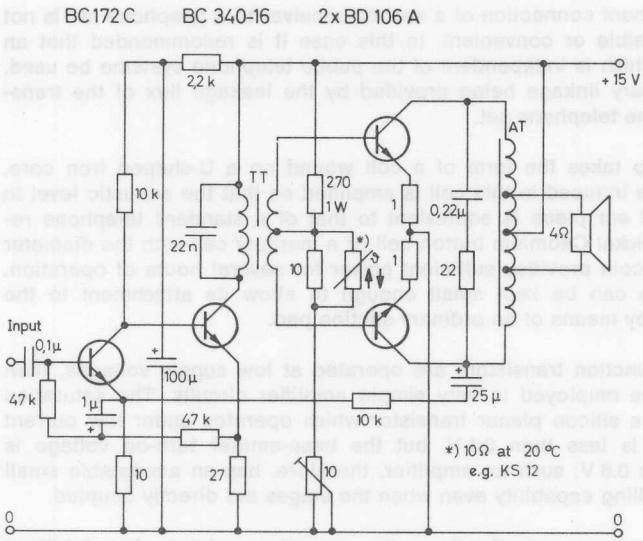
Transformer-Coupled 8 W Push-Pull Class B Amplifier

There are not many applications now for transformer-coupled push-pull amplifiers, these having been replaced by transformerless series push-pull amplifiers of the type described previously, which usually give a better performance. However, they are still required for some special applications. For example, a designer would have to fall back on a transformer-coupled amplifier design when there are supply voltage restrictions, and when a specified power level has to be supplied to a specified load. Use of an output transformer permits the amplifier to be matched to virtually any load, whereas in a series push-pull amplifier supply voltage, output power and load must be compatible.

The amplifier described operates from a 15 V supply and delivers 8 W into a 4 Ω load.

An auto-output transformer is used because it can be kept small and at the same time be designed to give a good LF response. The output stage incorporates a matched pair of NPN silicon planar transistors type BD 106 A, which function in a common emitter circuit and are fitted with 1 Ω emitter resistors for improved stability. The base bias divider for the output stage incorporates a 10 Ω preset control which permits the output transistor collector current to be set, as well as a thermistor (10 Ω at 20 °C) to provide temperature-compensation for the quiescent current. This current should be set to 50 mA when the output stage is cold and should be measured on a meter connected in the positive lead to the output transformer. Transistor BC 340 drives the output stage via transformer TT; the driver and the input transistor are directly coupled. Direct coupling offers the advantages of good frequency response, stable operating conditions, and component economy. Connected to the emitter of the input transistor BC 172 C is a 1 μF capacitor which reduces the effect of the 47 kΩ base resistor on the input impedance, this being increased to 100 kΩ.

Heavy negative feedback (approximately 10 dB) minimizes the effect of any transistor parameter spreads on the performance and reduces any distortion. Voltage negative feedback is used, the negative feedback voltage divider being formed by a 10 kΩ and a 10 Ω resistor. The division ratio of this divider determines the gain between the emitter of the input transistor and the collector of the output transistor (the transistor that provides a negative rather than positive feedback signal is best found by experiment), this being approximately 1000 ≙ 60 dB. The required input level for full output is consequently approximately 100 mV; the distortion at full output and at 1 kHz is approximately 1 %.



10. Transformer-coupled 8 W push-pull class B amplifier

Transformer Data

Driver transformer TT
Core: EI 42/14, type IV lamination with 2 x 0.1 mm air gap
Windings: Primary 900 turns 0.14 mm dia. en. copper wire
secondary 2 x 300 turns 0.22 mm dia. en. copper wire, bifilar wound

Output transformer AT
Core: EI 48/16, type IV lamination, alternately stacked
Windings: 100 + 50 + 50 + 100 turns 0.5 mm dia. en. copper wire, both halves bifilar wound

Telephone Pick-Up Amplifier

The permanent connection of a second receiver to a telephone set is not always feasible or convenient. In this case it is recommended that an amplifier which is independent of the public telephone systeme be used, the necessary linkage being provided by the leakage flux of the transformer in the telephone set.

The pick-up takes the form of a coil wound on a U-shaped iron core. The voltage induced in this coil is amplified so that the acoustic level in the second ear piece is equivalent to that of a standard telephone receiver. A Nickel Cadmium button cell or a mercury cell with the diameter of a small coin provides sufficient power for several hours of operation. The device can be kept small enough to allow its attachment to the telephone by means of an ordinary suction pad.

If silicon junction transistors are operated at low supply voltages, then they can be employed in very simple amplifier circuits. The saturation voltage of a silicon planar transistor which operates under low current conditions is less than 0.1 V, but the base-emitter turn-on voltage is higher than 0.6 V; such an amplifier, therefore, has an acceptable small signal handling capability even when the stages are directly coupled.

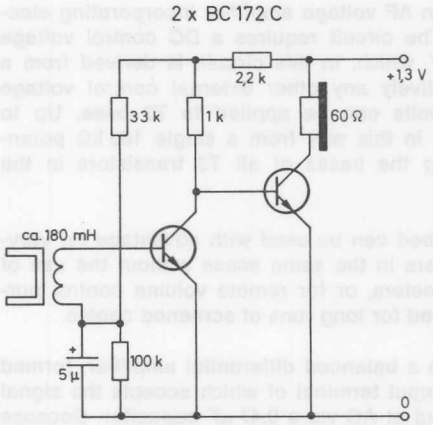
The low leakage current allows the operating point to be stabilized simply by connecting the base-bias divider to a tap on the collector load. Any increase in collector current then causes the base-emitter voltage to be reduced, with the result that the increase in collector current is opposed. The 5 μF capacitor is included to make this negative feedback arrangement ineffective at AC.

The pick up produces an average output of approximately 5 mV,this being amplified to a level of approximately 200 mV across the ear piece.

Coil Data

Core: Open U-core; approx. 5 x 5 mm^2 cross section and 15 mm leg length

Winding: 2000 turns 0.08 mm dia. en. copper wire



11. Telephone pick-up amplifier

Electronic Gain Control Circuit

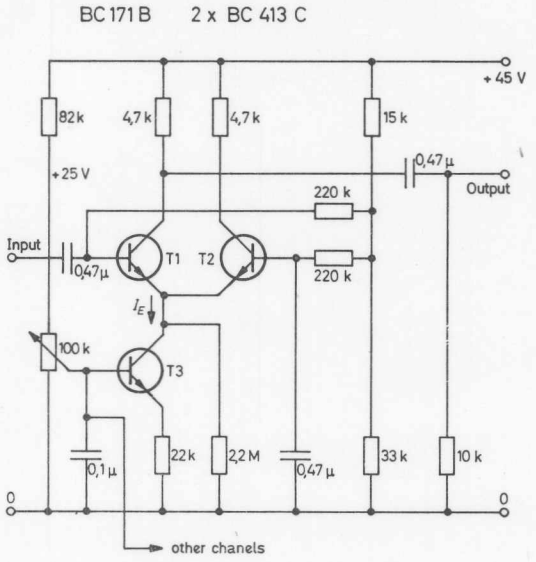
Fig. 12a shows the circuit of an AF voltage amplifier incorporating electronic gain control facilities. The circuit requires a DC control voltage variable between 0 and +25 V, which, in this circuit, is derived from a 100 kΩ potentiometer. Alternatively any other external control voltage variable between the same limits can be applied to T3 base. Up to 10 channels can be controlled in this way from a single 100 kΩ potentiometer, simply by connecting the bases of all T3 transistors in the channels to the potentiometer.

For example, the circuit described can be used with advantage for varying the gain of several amplifiers in the same sense without the use of mechanically ganged potentiometers, or for remote volume control purposes, thereby obviating the need for long runs of screened cables.

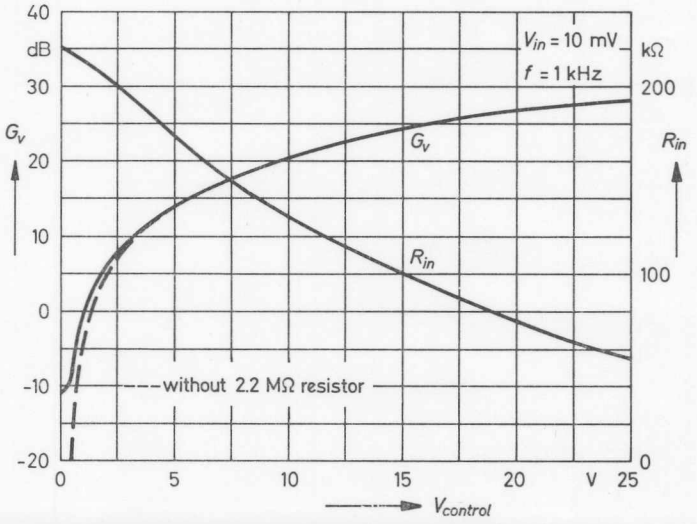
Basically, the circuit comprises a balanced differential amplifier, formed by transistors T1 and T2, one input terminal of which accepts the signal whilst the other one is grounded at AC via a 0.47 µF capacitor. Because the voltage gain of such a "long-tailed pair" is proportional to the emitter current I_E, this is set to the required value with the aid of a third transistor, T3, acting as a controlled constant current source.

The amplifier is designed to accept input levels up to 10 mV. At 10 mV input it has the following performance:

At +25 V control voltage	+28 dB
At 0 V control voltage	− 12 dB
Gain control range	40 dB
Input impedance	> 55 kΩ
Output impedance	< 10 kΩ
Lower cut-off frequency	< 30 Hz
Upper cut-off frequency	> 100 kHz
Change of voltage gain for ±10 % supply voltage variation	< 2 dB



12 a. Electronic gain control circuit



12 b. Voltage gain and input resistance plotted as a function of control voltage

III. Oscillators

Contents

III. 1.

RC Oscillator

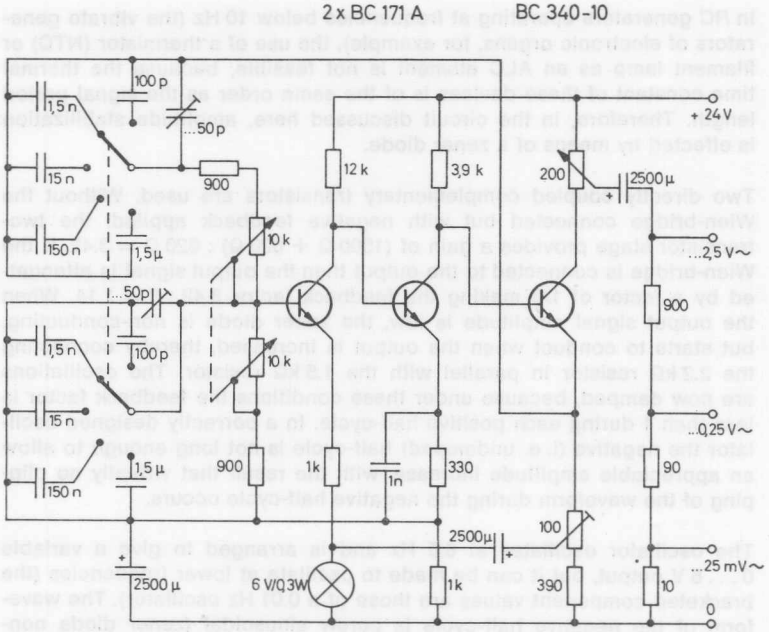
Oscillators incorporating a Wien-bridge as the frequency determining network have been successfully employed as sine-wave generators at frequencies up to 1 Megahertz and more. A Wien-bridge consists of two resistive and two complex arms, one complex arm being a series and the other one a parallel *RC* network. The voltage divider formed by these networks has a ratio of 1:3 at 'resonance'. In the circuit shown the resistive arm is formed by the emitter resistor of the last transistor and a filament lamp, which, because of its voltage-dependent resistance, acts as an automatic level control.

Connected across the 'detector' points of this bridge are the input terminals of a linear *RC*-coupled amplifier; this amplifier provides an output signal which is in phase with the input and is applied to the 'supply' terminals of the Wien-bridge.

There are two requirements for the maintenance of oscillations, namely an amplitude requirement and a phase requirement. The bridge output signal is only in phase with the bridge input signal at one particular frequency – the resonant frequency. At this frequency the two complex arms introduce an attenuation of 1:3. This means that, in theory, a voltage gain of 3 would be adequate to satisfy the amplitude requirement. The amplifier has a higher gain, however, this being reduced to the required factor of 3 by negative feedback.

Three directly coupled transistor stages, two of which function in common emitter configuration, are employed in the maintaining amplifier. The last stage acts as a 'split-load' stage, an amplified signal being taken from the emitter as well as from the collector. The emitter signal, which is in phase with the input voltage, is applied to the Wien-bridge, whilst the output voltage is taken from a 200 Ω potentiometer in the collector circuit. Because the take off point for the feedback signal is almost completely isolated from that for the output signal, any output load variations have virtually no effect on gain, distortion, or frequency of oscillation. All amplifier stages function with heavy DC negative feedback to stabilize the operating conditions. Leaving the emitter resistors unbypassed introduces, at the same time, negative AC feedback.

A large negative feedback signal is derived from the 100 Ω potentiometer in the emitter circuit of the last stage. This is applied to the filament lamp in the emitter circuit of the first stage, the lamp functioning as a signal amplitude stabilizing element. The 100 Ω preset control is used to adjust the amount of negative feedback, and hence the amplitude of the output signal.



1. *RC* Oscillator

In the circuit described the total frequency range of 10 Hz to 1 MHz is covered in five subranges, this being effected by the switching of the Wien-bridge capacitors. Two ganged potentiometers permit continuous varitation of frequency.

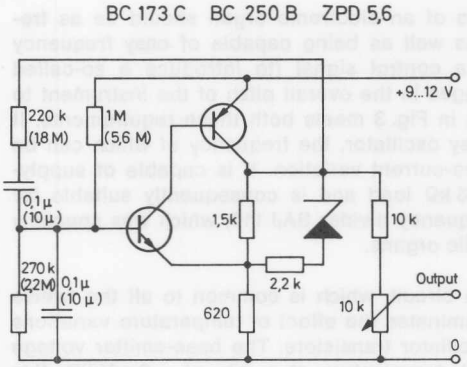
The output level is 2.5 V in the 10 Hz to 1 MHz frequency range with less than 0.2 % distortion at 1 kHz; the current consumption is approximately 35 mA.

RC Oscillator for Very Low Frequencies

In *RC* generators operating at frequencies below 10 Hz (the vibrato generators of electronic organs, for example), the use of a thermistor (NTC) or filament lamp as an ALC element is not feasible, because the thermal time constant of these devices is of the same order as the signal period length. Therefore, in the circuit discussed here, amplitude stabilization is effected by means of a zener diode.

Two directly coupled complementary transistors are used. Without the Wien-bridge connected but with negative feedback applied, the two-transistor stage provides a gain of (1500 Ω + 620 Ω) : 620 Ω = 3.42. If the Wien-bridge is connected to the output then the output signal is attenuated by a factor of 1/3 making the feedback factor 3.42 : 3 = 1.14. When the output signal amplitude is low, the zener diode is non-conducting, but starts to conduct when the output is increased, thereby connecting the 2.2 kΩ resistor in parallel with the 1.5 kΩ resistor. The oscillations are now damped, because under these conditions the feedback factor is less than 1 during each positive half-cycle. In a correctly designed oscillator the negative (i. e. undamped) half-cycle is not long enough to allow an appreciable amplitude increase, with the result that virtually no clipping of the waveform during the negative half-cycle occurs.

The oscillator oscillates at 6.5 Hz and is arranged to give a variable 0 . . . 6 V output, but it can be made to oscillate at lower frequencies (the bracketed component values are those of a 0.01 Hz oscillator). The waveform of the negative half-cycle is purely sinusoidal (zener diode non-conducting), but the waveform of the positive half-cycle is slightly inclined towards the right so that the phase angle of the peak differs by approximately 15° from that of a true sine wave. This, however, is acceptable in many applications (in a vibrato generator, for example). The oscillator has a current consumption of approximately 3 mA.



2. *RC* Oscillator for very low frequencies

LC Oscillator for Electronic Organs

The twelve master oscillators of an electronic organ should be as frequency-stable as possible, as well as being capable of easy frequency variation by application of a control signal (to introduce a so-called vibrato effect, or permit changes in the overall pitch of the instrument to be made). The circuit shown in Fig. 3 meets both these requirements. It is basically a modified Hartley oscillator, the frequency of which can be altered (within limits) by base-current variation. It is capable of supplying more than 6 V_{pp} into a 6 kΩ load and is consequently suitable for driving an ITT integrated frequency divider SAJ 110, which was specially developed for use in electronic organs.

A temperature compensation circuit, which is common to all the twelve master oscillators, largely eliminates the effect of temperature variations on the parameters of the oscillator transistors. The base-emitter voltage of transistor T3 changes with temperature at a rate of -2 mV/°C; this voltage is amplified, and is used to shift the base current of transistor T1 in the oscillator so that any frequency change caused by the same temperature variation is largely cancelled.

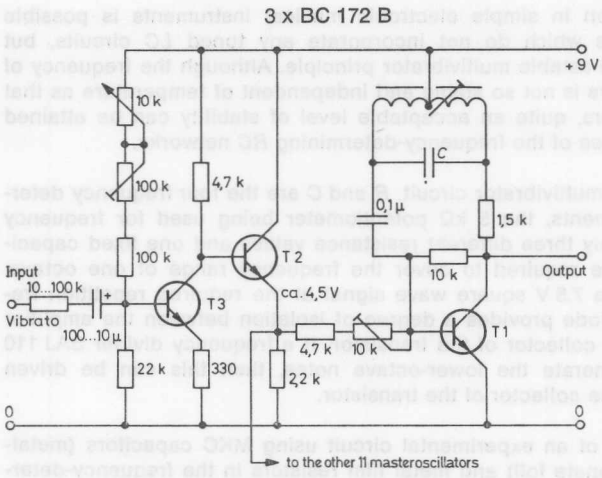
The compensation circuit also amplifies the vibrato AC signal, which is applied to T3 base via a series resistor and coupling capacitor. To adjust the circuit, first set the 10 kΩ potentiometer to mid-position, and then adjust the 100 kΩ preset control so that the emitter voltage of T2 is approximately 4.5 V. Adjustment of the 10 kΩ potentiometer should now permit the frequencies of all the 12 master oscillators to be increased or decreased simultaneously by a small amount, allowing the organ pitch to be matched to that of other instruments.

The 10 kΩ potentiometer in the T1 base circuit should be set so that the relative frequency deviation of each master oscillator is the same for a given vibrato signal amplitude. According to the equation

$$\Delta f = \pm f_o \cdot (\sqrt[12]{2} - 1),$$

a 1 V_{pp} vibrato signal applied to T3 base produces a frequency deviation equivalent to ±1 semitone. The value of the vibrato input resistor and that of the coupling capacitor depends on the magnitude of the vibrato voltage available.

In the following table component values for resonant circuits suitable for two different master octaves are given. The winding data apply to Vogt type 2349.1 coil assemblies.



3. *LC* Oscillator for electronic organs

For 6-leger octave (approx. 8 . . . 16 kHz) W = 1500 turns 0.1 mm dia. en. copper wire, centre tapped		For 5-leger octave (approx. 4 . . . 8 kHz) W = 2000 turns 0.1 mm dia.en. copper wire, centre tapped	
Pitch	Capacitor C	Pitch	Capacitor C
$c^6 \ldots d\#^6$	18 nF	$c^5 \ldots d\#^5$	33 nF
$e^6 \ldots g^6$	10 nF	$e^5 \ldots g^5$	18 nF
$g\#^6 \ldots b^6$	4.7 nF	$g\#^5 \ldots b^5$	10 nF
or			
$c^6 \ldots f^6$	15 nF	$c^5 \ldots f^5$	22 nF
$f\#^6 \ldots b^6$	6.8 nF	$f\#^5 \ldots b^5$	12 nF

The frequency of the master oscillators varies by not more than ± 0.2 % at ambient temperatures from 0 to +60 °C. This assumes that a stabilized power supply is used.

RC Oscillator for Simple Electronic Musical Instruments

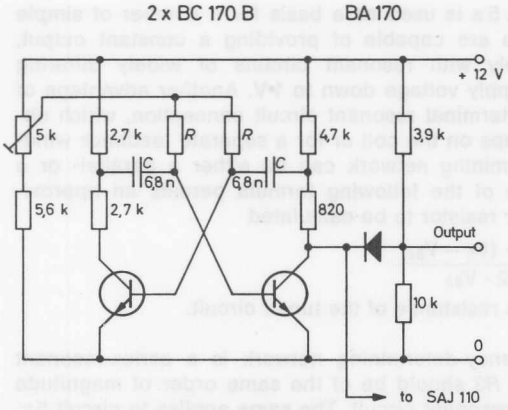
Tone generation in simple electronic musical instruments is possible with oscillators which do not incorporate any tuned *LC* circuits, but function on the astable multivibrator principle. Although the frequency of these oscillators is not so stable and independent of temperature as that of *LC* oscillators, quite an acceptable level of stability can be attained by correct choice of the frequency-determining *RC* networks.

In this astable multivibrator circuit, *R* and *C* are the four frequency determining components, the 5 kΩ potentiometer being used for frequency adjustment. Only three different resistance values and one fixed capacitance value are required to cover the frequency range of one octave. The output is a 7.5 V square wave signal at the required repetition frequency. The diode provides a degree of isolation between the amplifier output and the collector of the transistor. If a frequency divider SAJ 110 is used to generate the lower-octave notes, then this can be driven directly from the collector of the transistor.

The frequency of an experimental circuit using MKC capacitors (metallized polycarbonate foil) and metal film resistors in the frequency-determining *RC* networks varied by less than 0.5 % over the temperature range +10 to +40 °C. The oscillator, which draws approximately 7 mA of current, requires a stabilized power supply.

The three tuning resistance values listed below were found by experiment, and are all that is required to generate the 12 notes of an octave:

c♯(554 Hz) . . . e (659 Hz)	150 kΩ ±5 %
f (698 Hz) . . . g♯(831 Hz)	180 kΩ ±5 %
a (880 Hz) . . . c (1047 Hz)	240 kΩ ±5 %



4. *RC* Oscillator for simple electronic musical instruments

Two-Terminal Oscillator Circuits

The circuit shown in Fig. 5a is used as a basis for a number of simple oscillator variants. These are capable of providing a constant output, and will oscillate reliably with resonant circuits of widely differing dynamic resistance at supply voltage down to 1 V. Another advantage of these circuits is the two-terminal resonant circuit connection, which obviates the need for any taps on the coil or for a separate feedback winding. The frequency-determining network can be either a parallel- or a series tuned circuit. Use of the following formula permits an approximate value for the emitter resistor to be calculated

$$R_1 \approx \frac{R_{res} \cdot (V_S - V_{BE})}{2 \cdot V_{BE}}$$

where R_{res} is the dynamic resistance of the tuned circuit.

In circuit 5b. the frequency-determining network is a series-resonant circuit. Resistors *R2* and *R3* should be of the same order of magnitude as the ESR of the series-resonant circuit. The same applies to circuit 5c. where a crystal rather than a series-resonant circuit is used. Capacitor *C* allows the oscillator frequency to be pulled on to the nominal crystal frequency.

Circuit 5d. is a variant of an astable multivibrator. The frequency of oscillation is approximately

$$f \approx \frac{400}{R \cdot C} \text{ kHz } (\text{k}\Omega, \text{nF})$$

where $R = R2 + R3$. Also, the following conditions must be satisfied:

$$R3 > R2$$

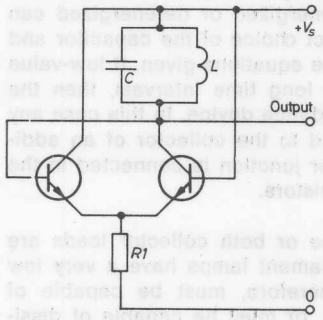
$$R3 < 0.2 \cdot h_{FE} \cdot R2,$$

$$\frac{2\,(V_S - V_{BE})}{R1} \approx \frac{V_{BE}}{R2},$$

where h_{FE} is the DC current gain of the left-hand transistor under the chosen operating conditions.

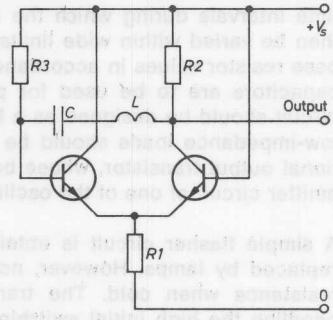
Matched transistors, or at least transistors of the same type with similar current gains, should be employed in all four circuits.

e.g. BC 170



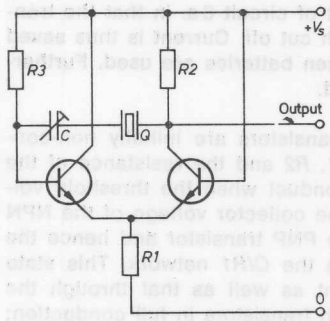
5 a. Oscillator with parallel resonant circuit

e.g. BC 170



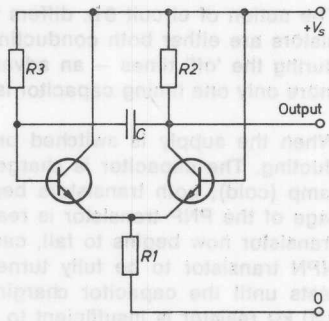
5 b. Oscillator with series resonant circuit

e.g. BC 170



5 c. Crystal oscillator

e.g. BC 170



5 d. Astable multivibrator

Flasher Circuits

The multivibrator discussed in IV. 4. can be used as a repetitive timer – one of the collector loads can be replaced by a relay, for example. The time intervals during which the relay is energized or de-energized can then be varied within wide limits by correct choice of the capacitor and base resistor values in accordance with the equations given. If low-value capacitors are to be used for producing long time intervals, then the circuit should be designed as a high-impedance device. In this case any low-impedance loads should be connected to the collector of an additional output transistor, whose base-emitter junction is connected in the emitter circuit of one of the oscillator transistors.

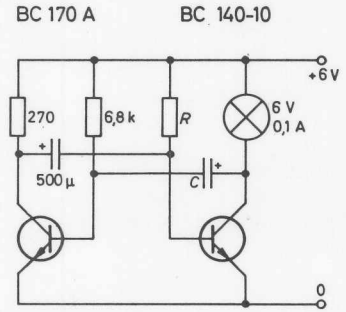
A simple flasher circuit is obtained if one or both collector loads are replaced by lamps. However, note that filament lamps have a very low resistance when cold. The transistor, therefore, must be capable of handling the high initial switching current, or must be capable of dissipating the power produced when it is non-saturated at the instant of switch-on.

Circuit 6 a. incorporates a lamp, the on/off ratio of which can be adjusted by variation of the R and C values. If $C = 50\ \mu F$ and $R = 2.7\ k\Omega$, then the 'on' time is approximately 0.3 s and the 'off' time is approximately 1 s.

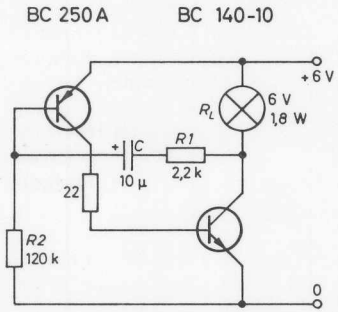
The action of circuit 6 b. differs from that of circuit 6 a. in that the transistors are either both conducting or both cut off. Current is thus saved during the 'off' times – an advantage when batteries are used. Furthermore only one timing capacitor is required.

When the supply is switched on both transistors are initially non-conducting. The capacitor is charged via *R1*, *R2* and the resistance of the lamp (cold); both transistors begin to conduct when the threshold voltage of the PNP transistor is reached. The collector voltage of the NPN transistor now begins to fall, causing the PNP transistor and hence the NPN transistor to be fully turned on via the *C/R1* network. This state lasts until the capacitor charging current as well as that through the 120 kΩ resistor is insufficient to hold both transistors in full conduction; the circuit then flips back to the cut-off condition.

The 'on' time of the lamp is determined by the time constant $\tau_{on} = R1 \cdot C$, and the 'off' time by $\tau_{off} = (R1 + R2) \cdot C$, the 'off' time being consequently always longer than the 'on' time. The value of *R2* must be chosen so that condition $R2 > h_{FE\,1} \cdot h_{FE\,2} \cdot R_L$ is satisfied, i. e. it must exceed the product of the DC current gains of both transistors times the lamp resistance.

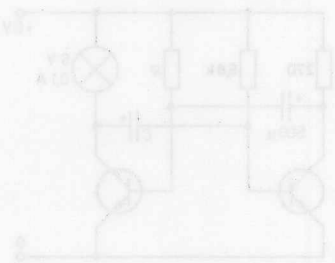


6 a. Conventional multivibrator flasher circuit



6 b. Complementary multivibrator flasher circuit

Little practical value attaches to circuit 6 b., because the current gains of both transistors are subject to spreads, and it is difficult, therefore, to repeat the circuit performance with different transistors.



IV. Digital and Pulse Circuits

Contents

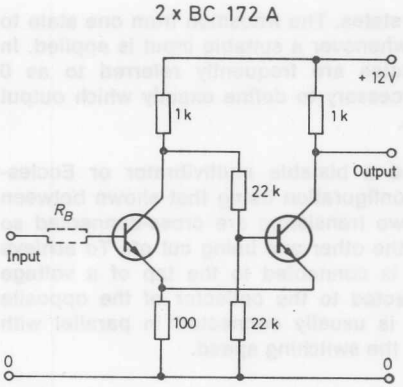
Schmitt Trigger

A Schmitt trigger is a simple switching circuit, whose output can be in only one of two states, depending on the magnitude of the input signal. If the input is low, then the lefthand transistor is cut-off and the one on the right conducts. The potential at the output depends on the collector to emitter resistor ratio, and is approximately $^1/_{11}$th of the supply voltage. If the input voltage is increased, then this potential undergoes initially no change, the change-over point being reached only when the input potential exceeds the voltage dropped across the common emitter resistor plus the threshold voltage of the lefthand transistor, which now begins to conduct. The lefthand collector potential consequently falls and the righthand transistor starts to cut off. This has the effect of initially reducing the current through the common emitter resistor and therefore also the voltage dropped across it, with the result that the base-emitter voltage of the lefthand transistor now increases. The whole action is cumulative until a state is reached in which the lefthand transistor conducts and the one on the right is cut off; the output is now at supply potential.

The circuit remains in this state until the input voltage is reduced again to below a certain level, whereupon the states of the two transistors are reversed in a similar way to that described above.

The difference between the switching level associated with a rising input and that associated with a falling input is called the hysteresis voltage V_{HY}. This is affected, among other things, by the threshold voltage of the lefthand transistor as well as by the value of the base resistor R_B. For example, in the circuit shown, $V_{HY} \approx 0.6\,V$ if $R_B = 0$ (voltage drive condition), and is approximately $0.2\,V$ if $R_B = 15\,k\Omega$. However, the base resistor R_B (which is assumed to include also the drive-source resistance) cannot be increased indefinitely. The voltage drop due to the base current of the lefthand transistor should not exceed the hysteresis voltage (measured under voltage drive conditions), otherwise the circuit would cease to function as a switch and would merely act as an amplifier.

If the output of the Schmitt trigger is to drive an NPN transistor whose emitter is connected to the zero line, then it is advisable to use a zener diode as a coupling component. It is also possible to pass the collector current of the righthand transistor through the base-emitter junction of a PNP transistor.



1. Schmitt trigger

Bistable Flip-Flop

A bistable flip-flop has two stable states. The transition from one state to the other is very fast and occurs whenever a suitable input is applied. In digital engineering these two states are frequently referred to as 0 (nought) and 1 (one), and it is necessary to define exactly which output level is associated with what state.

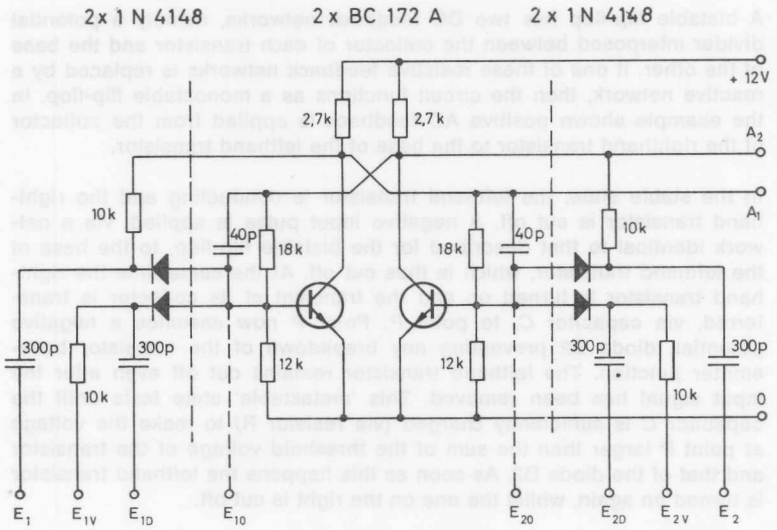
A bistable flip-flop is also called a bistable multivibrator or Eccles-Jordan circuit, the basic circuit configuration being that shown between the two dotted lines in Fig. 2a. Two transistors are cross-connected so that only one conducts at a time, the other one being cut off. To achieve this, the base of each transistor is connected to the tap of a voltage divider, each divider being connected to the collector of the opposite transistor. A low-value capacitor is usually connected in parallel with each coupling resistor to increase the switching speed.

The circuit has two inputs E_{10} and E_{20}, and two complementary outputs A_1 and A_2. Let us assume that the circuit is in the 1-state when output A_1 is positive and that it is in the 0-state when A_1 is at zero potential.

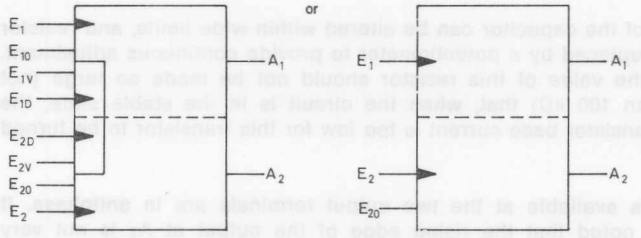
Flip-flops are usually switched by pulses which cause the transistor that is conducting at the time to be cut off. In order to ensure correct operation, each input is, therefore, preceded by input networks comprising diodes, capacitors and resistors. These components (shown to the left and right of the dotted lines) form pulse gates with AC inputs E_1 and E_2 which, if necessary, can be connected together to form a single input-steering network. In this case the circuit changes state only on application of a negative pulse. The gates ensure that the negative drive pulse is always steered to the base of that transistor which is conducting at the time. This is because the cathode of the diode in the base circuit of this transistor is connected, via a 10 kΩ resistor, to its collector, so that virtually no reverse bias is applied to it. The negative pulse is consequently transferred to the base of this transistor.

In the network preceding the transistor that is cut off, however, the cathode of the diode is connected, via the 10 kΩ resistor, to almost the full supply voltage and is consequently reverse-biased. Any negative pulse lower in amplitude than the supply voltage is therefore effectively isolated from the base and thus unable to interfere with the turn-on process of the cut off transistor.

Some digital circuits require additional inputs; circuit 2a, therefore, shows two more AC inputs E_{1D} and E_{2D} and the two associated gating inputs E_{1V} and E_{2V}. Any input pulses applied to either E_{1D} or E_{2D} will switch the circuit only if the associated gating input terminal is at 0 potential; if this potential is positive, then the input is inhibited.



2 a. Bistable flip-flop



2 b. Block diagram symbol for bistable flip-flop

Fig. 2b. shows the block circuit diagram symbol of a bistable flip-flop, the input and output designations being the same as those employed in Fig. 2a. In all the examples that follow only the symbols shown in 2b. will be used.

Monostable Flip-Flop

A bistable flip-flop has two DC feedback networks, namely a potential divider interposed between the collector of each transistor and the base of the other. If one of these resistive feedback networks is replaced by a reactive network, then the circuit functions as a monostable flip-flop. In the example shown positive AC feedback is applied from the collector of the righthand transistor to the base of the lefthand transistor.

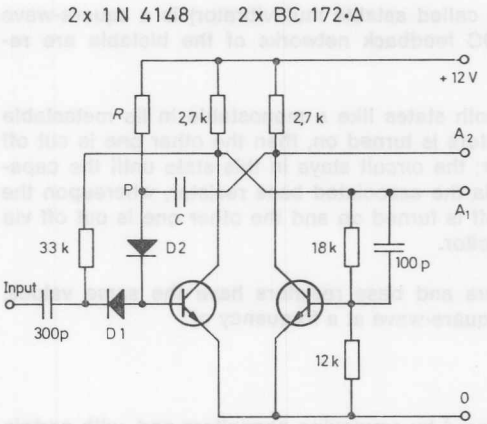
In the stable state, the lefthand transistor is conducting and the right-hand transistor is cut off. A negative input pulse is applied, via a network identical to that described for the bistable flip-flop, to the base of the lefthand transistor, which is thus cut off. At the same time the right-hand transistor is turned on and the transient at its collector is transferred, via capacitor *C,* to point P. Point P now assumes a negative potential, diode D2 preventing any breakdown of the transistor base-emitter junction. The lefthand transistor remains cut off even after the input signal has been removed. This 'metastable' state lasts until the capacitor *C* is sufficiently charged (via resistor R*)* to make the voltage at point P larger than the sum of the threshold voltage of the transistor and that of the diode D2. As soon as this happens the lefthand transistor is turned on again, whilst the one on the right is cut off.

The time, t_m, during which the monostable is in the metastable state, depends on the value of capacitor *C* and that of the charging resistor *R,* i. e. $t_m \approx 0.7\ RC$, a 250 µF capacitor and an 18 kΩ discharge resistor giving a time of $t_m = 3.15$ s.

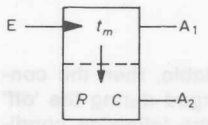
The value of the capacitor can be altered within wide limits, and resistor *R* can be replaced by a potentiometer to provide continuous adjustment. However, the value of this resistor should not be made so large (not greater than 100 kΩ) that, when the circuit is in the stable state, the lefthand transistor base current is too low for this transistor to be turned fully on.

The signals available at the two output terminals are in antiphase. It should be noted that the rising edge of the output at A_2 is not very steep; this is because, after the righthand transistor has been cut off, some time elapses before *C* is charged.

In the following circuit diagrams, the simplified monostable symbol shown in Fig. 3b is used, the switching time t_m and the required *R* and *C* values being printed inside the block.



3 a. Monostable flip-flop



3 b. Block diagram symbol for monostable flip-flop

Astable Flip-Flop

The astable flip-flop (also called astable multivibrator) is a square-wave generator in which the DC feedback networks of the bistable are replaced by *RC* networks.

The circuit functions in both states like a monostable in its metastable state. If one of the transistors is turned on, then the other one is cut off via the coupling capacitor; the circuit stays in this state until the capacitor is reverse-charged via the associated base resistor, whereupon the transistor previously cut off is turned on and the other one is cut off via the second coupling capacitor.

If both coupling capacitors and base resistors have the same values, then the output is a 1 : 1 square-wave at a frequency of

$$f \approx \frac{0.7}{R_B \cdot C}$$

The duty factor can be altered by employing capacitors and, with certain limiiations, resistors of unequal values. The 'on' times of transistors T1 and T2 are given by

$$t_1 \approx 0.7\ R_{B1} \cdot C1 \text{ and } t_2 \approx 0.7\ R_{B2} \cdot C2.$$

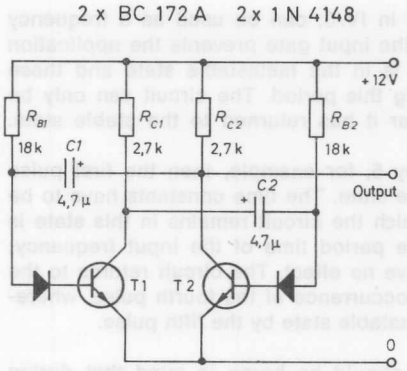
The frequency is then

$$f = \frac{1}{t_1 + t_2}$$

If the two 'on' times are to be independently adjustable, then the conditions must be such that each capacitor is fully charged during the 'off' periods via the collector resistors. To achieve this the following conditions must be satisfied:

$$t_1 > 3R_{C2} \cdot C1 \text{ and } t_2 > 3R_{C1} \cdot C2.$$

If required, the fixed base resistors can be replaced by variable ones to provide continuous 'on' period adjustment. But to ensure correct functioning of the circuit, the value of these resistors must not be too high, otherwise the base current becomes too low and the transistors are not fully turned on.



4. Astable flip-flop

The following upper limit constraints apply:

$$R_{B1} < 0.5 \cdot h_{FE} \cdot R_{C1} \text{ and } R_{B2} < 0.5 \cdot h_{FE} \cdot R_{C2},$$

where h_{FE} is the minimum DC current gain at the operating collector current. If the values of these base resistors are made too low, then oscillations may not start on application of the supply voltage, due to the fact that both transistors are immediately turned fully on. The following constraints apply:

$$R_{B1} > 10 \cdot R_{C1} \text{ and } R_{B2} > 10 \cdot R_{C2}.$$

Using the component values shown, the multivibrator oscillates at approximately 10 Hz.

Monostable Frequency Divider Chain

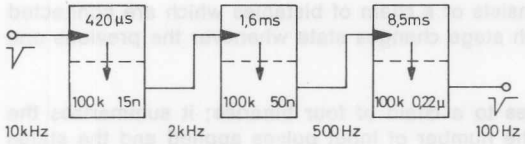
The monostable circuit discussed in IV. 3. can be used as a frequency divider. This is possible because the input gate prevents the application of input pulses whilst the circuit is in the metastable state and these are consequently ineffective during this period. The circuit can only be retriggered by an input pulse after it has returned to the stable state.

If a frequency is to be divided by 5, for example, then the first pulse trips the circuit into the metastable state. The time constants have to be chosen so that the time during which the circuit remains in this state is slightly longer than four times the period time of the input frequency; the next four input pulses then have no effect. The circuit returns to the stable state only briefly, after the occurrence of the fourth pulse, whereupon it is tripped again to the metastable state by the fifth pulse.

When designing such a circuit it should be borne in mind that during the interval between the return to the stable state and the arrival of the next pulse, capacitor *C* must be charged via the collector resistor of the righthand transistor.

The maximum division ratio attainable with such a divider stage depends to a large extent on component tolerances as well as on component ageing and temperature characteristics; supply voltage variations also affect the switching time. Division ratios between 5 and 7 are quite feasible without the need for any special circuit arrangements.

If required, several of these dividers can be cascaded. The block diagram shows how a pulse frequency of 10 kHz can be divided by $5 \cdot 4 \cdot 5 = 100$, using three cascaded dividers. The required timing network component values are printed inside the blocks. The resistors *R* should be made variable so that the stages can be set to the required period times.



5. Monostable frequency divider chain

Binary Counter

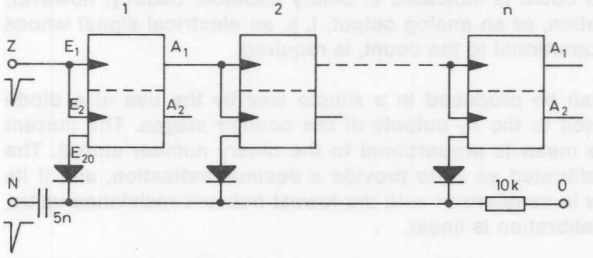
The binary counter consists of a chain of bistables which are connected in such a way that each stage changes state whenever the previous one changes from '1' to '0'.

The table below applies to a chain of four binaries; it summarizes the relationship between the number of input pulses applied and the states of the individual bistables. As can be seen, if the states of the stage are considered as binary numbers, then they give the count in binary notation. Each counting stage is initially at '0'. The first input pulse sets the first stage to '1'. The second input pulse returns the first stage to '0' and causes the second stage to be switched to '1'; this count corresponds to binary 2. The next pulse trips the first stage to '1' again and the count now corresponds to binary 3.

As shown in the table, there are 16 different combinations for four counting stages (0 . . . 15) and, in general, an n-stage counter can count up to 2^n.

Fig. 6 shows the block diagram of a binary counter incorporating the bistables discussed in IV. 2. The complete chain of bistables can be reset to zero by application of a negative pulse to input N. The pulses to be counted are applied to input Z, and complementary logic outputs are available from terminals A_1 and A_2.

All diodes: 1 N 414 8



6. Binary counter

Signal at A_1 output of counter stages				Pulse count
4	3	2	1	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Digital-Analog Converter for Binary Counters

If the outputs of the individual binaries are used to energize lamps, then the accumulated count is indicated in binary notation. Usually, however, a decimal indication, or an analog output, i. e. an electrical signal whose magnitude is proportional to the count, is required.

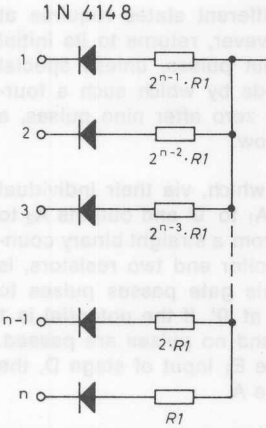
Such a signal can be produced in a simple way by the use of a diode network connected to the A_2 outputs of the counter stages. The current indicated on the meter is proportional to the binary number stored. The meter can be calibrated so as to provide a decimal indication, and if its resistance is low in comparison with the lowest network resistance value, then the scale calibration is linear.

The converter supply voltage should not exceed approximately 80 % of the counter supply voltage to ensure that for a count of zero the meter reading is zero.

Resistor *R1* can be calculated by use of the formula

$$R1 = \frac{2\,V_S}{I}$$

where the current *I* is the FSD sensitivity of the meter.



7. Digital-analog converter for binary counters

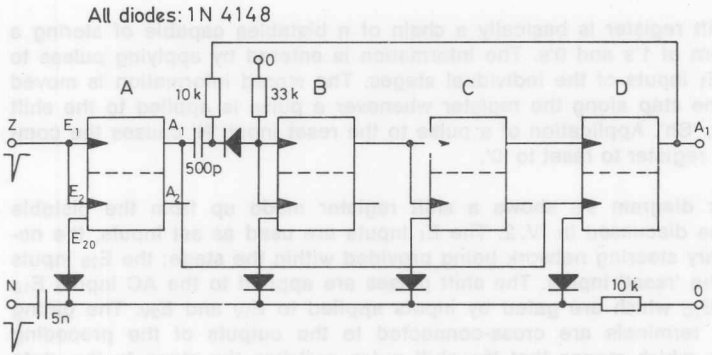
Decade Counter with Binary Stages

A binary counter capable of assuming ten different states requires at least four bistable stages. Such a counter, however, returns to its initial state after more than 10, namely $2^4 = 16$ input pulses, unless special measures are taken. There are several methods by which such a four-stage binary counter can be made to reset to zero after nine pulses, a particularly simple method being described below.

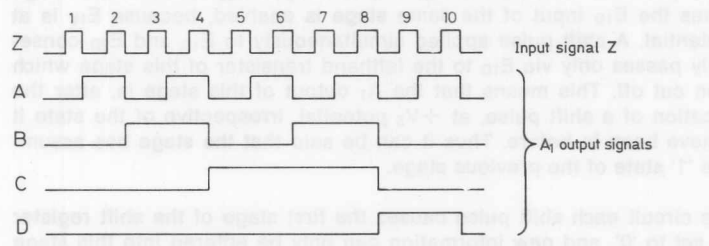
Block diagram 8a shows four bistable stages which, via their individual reset inputs E_{20}, can be reset to zero (outputs A_1 to '0' and outputs A_2 to '1') from input N. However, this circuit differs from a straight binary counter in that a gate, comprising a diode, a capacitor and two resistors, is interposed between stage A and stage B. This gate passes pulses to stage B only when the A_1 output of stage D is at '0'. If the potential is 1 ($+V_S$), then the gate diode is reverse biased and no pulses are passed. The A_1 output of stage C is applied only to the E_1 input of stage D, the E_2 input for stage D being the A_1 output of stage A.

Let us assume that all stages are initially at '0'. The gate interposed between stages A and B is then open and the counter counts like a normal binary counter while stage D is at '0', this condition being maintained until the eighth input pulse is applied. Stage D now changes state, with the result that the gate is closed and stages B and C consequently retain their '0' state. The ninth pulse switches stage A from '0' to '1' and the tenth pulse switches it from '1' back to '0'. The resultant transient, although not passed to stage B, causes stage D to be switched to '0', via input E_2, so that, after the ninth input pulse, all stages are once more at '0'.

Multi-decade counters are easily constructed simply by cascading several of the four-stage decades described, the A_1 output of stage D being connected to the input of the next decade.



8a. Decade counter with binary stages



8b. Pulse diagram

Shift Register

A shift register is basically a chain of n bistables capable of storing a pattern of 1's and 0's. The information is entered by applying pulses to the E_1 inputs of the individual stages. The stored information is moved by one step along the register whenever a pulse is applied to the shift input, 'Sh'. Application of a pulse to the reset input 'N' causes the complete register to reset to '0'.

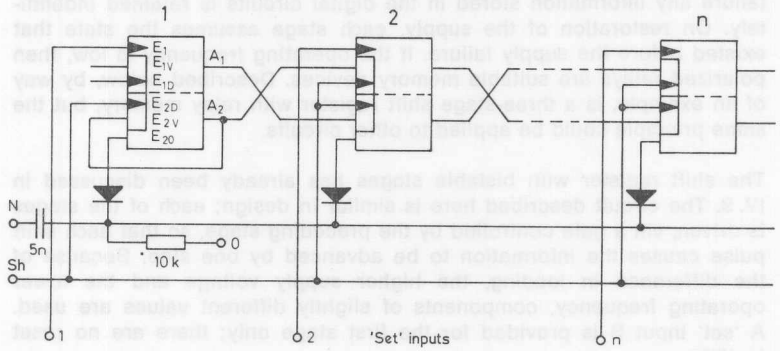
Block diagram 9a shows a shift register made up from the bistable stages discussed in IV. 2. The E_1 inputs are used as set inputs, the necessary steering network being provided within the stage; the E_{20} inputs are the 'reset' inputs. The shift pulses are applied to the AC inputs E_{1D} and E_{2D} which are gated by inputs applied to E_{1V} and E_{2V}. The gating input terminals are cross-connected to the outputs of the preceding stage, which means that the shift pulse switches the stage to the state previously assumed by the preceding stage.

To illustrate this, assume that one of the stages is in the '1' state, i. e. output A_1 is at $+V_S$ potential and output A_2 is at '0' potential. This positive A_1 potential inhibits via E_{2V} the AC input E_{2D} of the next stage whereas the E_{1D} input of the same stage is enabled, because E_{1V} is at '0' potential. A shift pulse applied simultaneously to E_{1D} and E_{2D} consequently passes only via E_{1D} to the lefthand transistor of this stage which is then cut off. This means that the A_1 output of this stage is, after the application of a shift pulse, at $+V_S$ potential, irrespective of the state it may have been in before. Thus it can be said that the stage has assumed the '1' state of the previous stage.

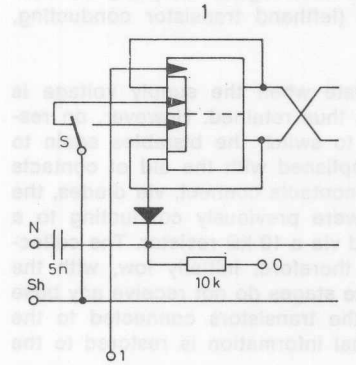
In this circuit each shift pulse causes the first stage of the shift register to be set to '0', and new information can only be entered into this stage via the E_1 input. Circuit 9b shows another version: Depending on the position of switch 'S', the information entered into the first stage on application of the shift pulse can be either a '0' or a '1'. Set and reset inputs (E_1 and E_{20} respectively) are also provided.

A shift register can also be arranged in the form of a ring, thereby causing the continuous circulation of any information pattern entered. To do this the E_{1V} and E_{2V} gating input terminals of the first stage must be cross-connected to the outputs of the final stage.

All diodes: 1 N 4148



9 a. Shift register



9 b. Setting of first stage by shift pulses

Shift Register with Polarized Relays Providing Information Storage on Supply Failure

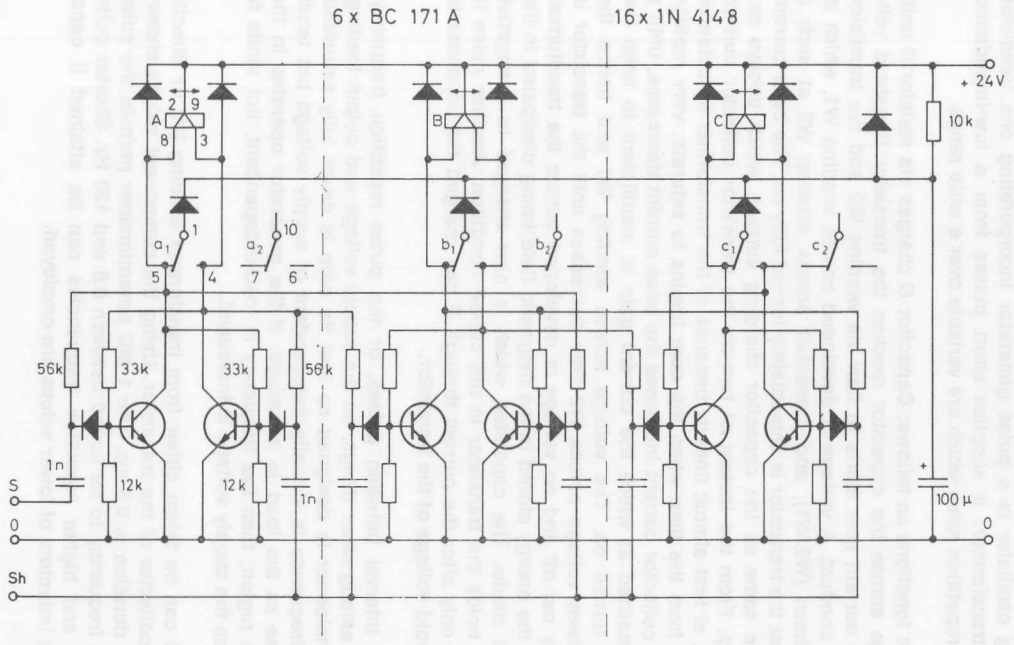
There are applications where it is necessary that in the event of a power failure any information stored in the digital circuits is retained indefinitely. On restoration of the supply, each stage assumes the state that existed before the supply failure. If the operating frequency is low, then polarized relays are suitable memory devices. Described below, by way of an example, is a three-stage shift register with relay memory, but the same principle could be applied to other circuits.

The shift register with bistable stages has already been discussed in IV. 9. The circuit described here is similar in design; each of the stages is driven, via a gate controlled by the preceding stage, so that each shift pulse causes the information to be advanced by one step. Because of the difference in loading, the higher supply voltage and the lower operating frequency, components of slightly different values are used. A 'set' input S is provided for the first stage only; there are no reset facilities.

Each polarized relay has two windings which form the collector loads of the individual stages. Three unused change-over contacts, a_2, b_2 and c_2, numbered 6, 7 and 10, are available as shift register outputs; the contacts are drawn in their '0' positions (lefthand transistor conducting, righthand transistor cut off).

These relays will not change their state when the supply voltage is removed and the stored information is thus retained. However, on restoration of the supply it is necessary to switch the bistables again to their previous states, this being accomplished with the aid of contacts a_1, b_1, c_1, numbered 1, 4 and 5. These contacts connect, via diodes, the collectors of those transistors which were previously conducting to a 10 μF capacitor, which is slowly charged via a 10 kΩ resistor. The collector voltages of these transistors are, therefore, initially low, with the result that the opposite transistors in the stages do not receive any base current, and stay cut off. Eventually the transistors connected to the capacitor are turned on and the original information is restored to the register.

Relay: Siemens V23018-D0011-A101 (coil resistance 1.1 kΩ).



10. Shift register with polarized relays providing information storage on supply failure

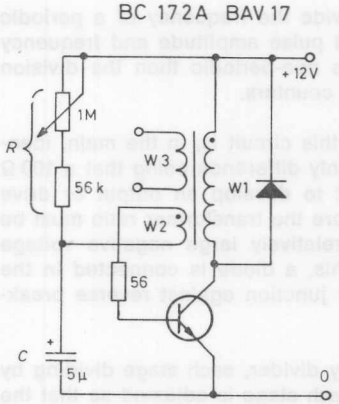
Blocking Oscillator

A blocking oscillator is a pulse generator incorporating one transistor and one transformer; it supplies short pulses from a low-impedance source at repetition rates which are variable over a wide range.

The circuit functions as follows: Capacitor *C* charges via resistor *R* until the voltage across the capacitor reaches the transistor threshold voltage; base current now starts to flow via winding W2 and the transistor begins to conduct. A voltage is developed across winding W1, which is stepped down (W2/W1), and presented across winding W2 at such a polarity that the transistor is immediately turned fully on. The base current is now the same as the capacitor charging current, which decays exponentially. From the instant of turn-on the transistor collector current increases, at first almost linearly because of the transformer inductance, and then, from the time when the core begins to saturate, very rapidly. While the collector current increases the base current decreases, until a point is reached at which the current gain is insufficient to keep the transistor turned on. The voltage across winding W1 and hence the stepped-down voltage across W2 now decreases until the transistor is completely cut off and no voltage is developed across the transformer windings, the energy stored in the magnetic field being dissipated in the free-wheel diode. The capacitor, which is now charged to a negative potential, holds the transistor in the cut-off condition. Another pulse is produced only after the current through *R* has charged the capacitor to the threshold voltage of the transistor.

The time interval between pulses, or the pulse repetition frequency, depends, among other things, on the supply voltage and output loading. If the transformer is designed so that its core is never fully saturated, then the frequency is virtually independent of supply voltage but tends to increase as the load is increased. If the generator operates in the saturation region, then the frequency is load-independent, but tends to increase as the supply voltage is increased.

An output can be taken either from transformer winding W3 or directly from the collector of the transistor. Using the component values shown, the pulse duration is 0.5 ms. The 1 MΩ potentiometer permits the pulse repetition frequency to be varied between 0.8 and 120 Hz. Shorter pulse durations and higher repetition frequencies can be attained if capacitors and inductors of lower values are employed.



11. Blocking oscillator

Transformer Data

Core: Ferrite cup core 22 mm dia. x 13 mm.
Windings: W1 = 300 turns 0.15 mm dia. en. copper wire
W2 = 150 turns 0.15 mm dia. en. copper wire
W3 as required

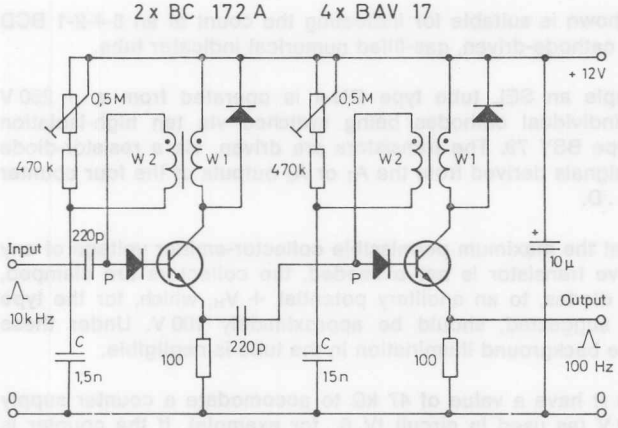
Blocking Oscillator Frequency Divider

Blocking oscillators may be used to divide the frequency of a periodic pulse sequence, provided that the input pulse amplitude and frequency stay constant. If the pulse sequence is non-periodic then the division can only be effected by means of binary counters.

The type of blocking oscillator used in this circuit is, in the main, identical with that described in IV. 11., the only difference being that a 100 Ω resistor is used in each emitter circuit to develop an output or drive signal for the following stage. Furthermore the transformer ratio must be made sufficiently large to produce a relatively large negative voltage across the base winding; because of this, a diode is connected in the base circuit to protect the base-emitter junction against reverse breakdown.

The circuit shows a two-stage frequency divider, each stage dividing by 10. The 0.5 MΩ potentiometer used in each stage is adjusted so that the period length of the signal produced by the free-running oscillator is slightly longer than 10 times the period length of the signal to be divided. Application of the signal then causes the blocking oscillator to be triggered every tenth input pulse, as described below: Immediately after the oscillator has produced a pulse, point P is at a negative potential which, because capacitor *C* is charged via the 470 kΩ resistor (and the potentiometer), increases exponentially. Superimposed on this rising voltage are the positive input pulses applied via the 220 pF capacitor. If the potentiometer is correctly adjusted, then the amplitude of any of the pulses up to the ninth is not high enough to trigger the blocking oscillator. Only during the 10th pulse does the positive peak voltage at this point exceed the sum of the transistor and diode threshold voltages, thereby causing the transistor to be turned on and a trigger pulse for the next stage to be produced.

The drive pulses should have an amplitude of approximately 5 V. It is also important that the output impedance of the power supply is low, because otherwise interaction could occur between stages; it is recommended that a 10 μF capacitor be connected across the supply rails. Supply voltage variations of up to ± 5 % are permissible, but, if these limits are exceeded, then the supply should be stabilized by means of a zener diode and series dropper.



12. Blocking oscillator frequency divider

Transformer Data

Core: M 20/5 laminations IV, alternately stacked
Windings: W1 = 200 turns 0.12 mm dia. en. copper wire
W2 = 600 turns 0.12 mm dia. en. copper wire

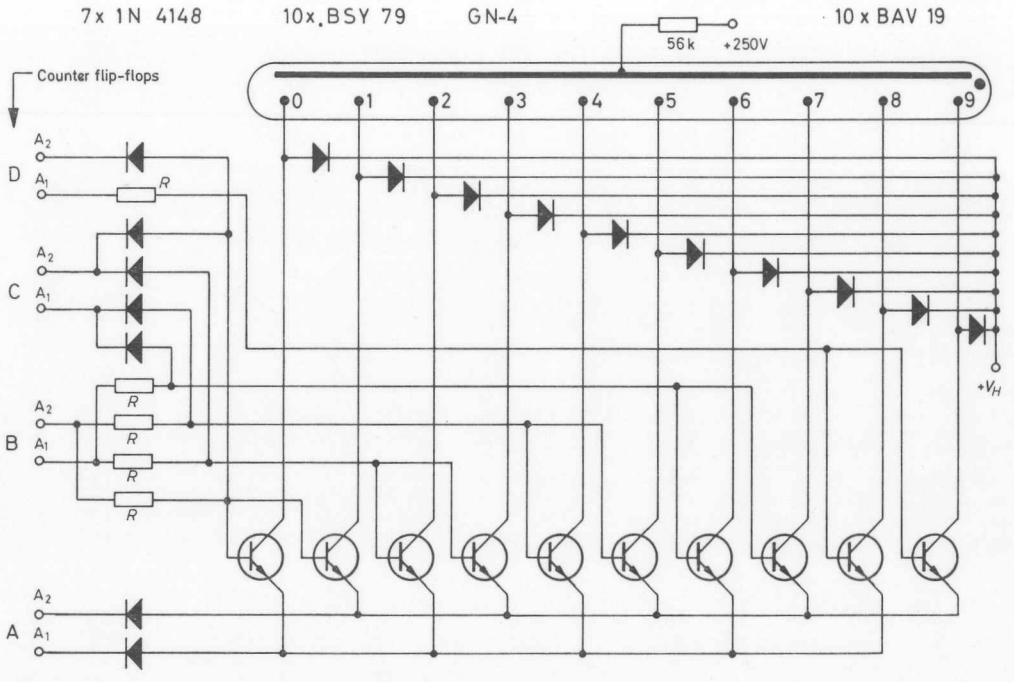
Numerical Indicator for BCD Counters

The circuit shown is suitable for indicating the count of an 8-4-2-1 BCD counter on a cathode-driven, gas-filled numerical indicator tube.

In this example an SEL tube type GN-4 is operated from a + 250 V supply, the individual cathodes being switched via ten high-isolation transistors type BSY 79. The transistors are driven, via a resistor-diode network, by signals derived from the A_1 or A_2 outputs of the four counter flip-flops A . . . D.

To ensure that the maximum permissible collector-emitter voltage of any non-conductive transistor is not exceeded, the collectors are clamped, by means of diodes, to an ancillary potential + V_H, which, for the type of transistor suggested, should be approximately 100 V. Under these conditions the background illumination in the tube is negligible.

The resistors *R* have a value of 47 kΩ to accomodate a counter supply voltage of 12 V (as used in circuit IV. 8., for example). If the counter is furnished by a standard 5 V supply (normally specified for integrated circuits), then *R* should be reduced to 10 kΩ.



13. Numerical indicator for BCD counters

V. Timer and Relay Circuits

Contents

Relay Pull-On Delay Circuit

Although a delay in the operation of a relay can be obtained simply by the use of capacitors, this is not a particularly good method if long or easily adjustable delay times are required. In this case it is more advantageous to energize the relay via a transistor which has an *RC* network connected to its base.

The threshold sensitivity of such a simple circuit is largely determined by the relay energizing and de-energizing voltages, and, since these are subject to spreads and other influences, the timing accuracy of such a circuit is rather poor.

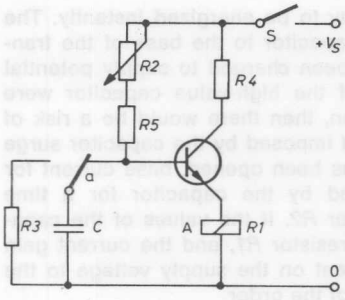
In the circuit shown the transistor base is connected, via a n. c. relay contact, to a capacitor which, when the starting switch is closed, causes a delay in the rise of base current. Potentiometer *R2* permits this delay to be adjusted. To eliminate any drop-out delay when switch S is opened, the capacitor is disconnected from the base by means of the change-over contact as soon as the relay is energized. The capacitor now discharges via the low-value contact protection resistor *R3*, so that the circuit is immediately ready for operating again. Resistor *R4* is included to restrict the power dissipated by the transistor.

If the supply voltage, the capacitance *C*, the current gain h_{FE}, and the required relay energizing power are known, then the only other parameter required is the relay coil resistance *R1*, and hence the relay operating voltage which gives the longest delay. This is governed by the time-constant

$$\tau = C \cdot \frac{R2_{max} \cdot h_{FE} \cdot R1}{R2_{max} + h_{FE} \cdot R1}$$

If a relay requiring an operating voltage slightly less than the supply voltage is chosen, then the maximum value of *R2* would have to be relatively low to permit sufficient base current to flow. If, on the other hand, a relay with an operating voltage very much lower than the supply voltage is chosen, then the coil resistance would have to be very low for the necessary pull-on power to be developed. In both instances the resistance of the parallel network $R2_{max} \,||\, h_{FE} \cdot R1$ would be low, with the additional disadvantage of low efficiency in the second instance.

The longest delay is attained if the relay operating voltage is 67 % of the supply voltage. In this case $R2_{max}$ would have to be made equal to $0.5\ h_{FE} \cdot R1$ and *R4* would have to be equal to $0.5 \cdot R1$. If the relay pull-on voltage is approximately 30 % less than the nominal operating voltage, then the maximum delay time is approximately equal to the time constant given above.



1. Relay pull-on delay circuit

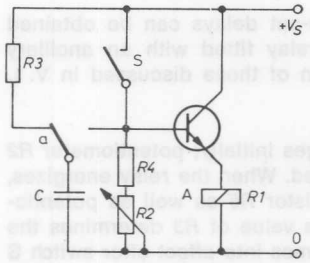
Relay Drop-Out Delay Circuit

Closure of the switch S causes the relay to be energized instantly. The change-over contact 'a' connects the capacitor to the base of the transistor, the capacitor having previously been charged to supply potential via the low-value series resistor *R3*. If the high-value capacitor were switched while in a discharged condition, then there would be a risk of relay chatter caused by the sudden load imposed by the capacitor surge current on the supply. After switch S has been opened, base current for the transistor continues to be supplied by the capacitor for a time governed by the setting of potentiometer *R2*. If the values of the capacitor *C*, the discharge resistor *R2*, coil resistor *R1*, and the current gain h_{FE} are fixed, then the delay is dependent on the supply voltage to the relay de-energizing voltage ratio and is of the order

$$\tau = C \cdot \frac{R2 \cdot h_{FE} \cdot R1}{R2 + h_{FE} \cdot R1}$$

Resistor *R4* is included to prevent the supply being short-circuited when *R2* is set to the minimum resistance position. The value of *R4* should be very much lower than that of *R2*.

As in the other circuit, the delay time is affected by the relay parameters and is subject to spreads, therefore.



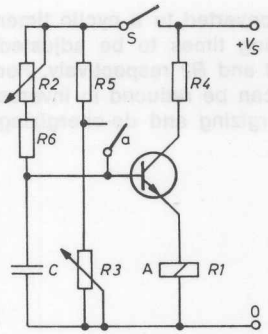
2. Relay drop-out delay circuit

Relay Pull-On and Drop-Out Delay Circuit

Independently adjustable pull-on and drop-out delays can be obtained with a transistor circuit incorporating a relay fitted with an ancillary contact 'a', the circuit being a combination of those discussed in V. 1. and V. 2.

When switch S is closed, capacitor *C* charges initially; potentiometer *R2* permits the pull-on delay time to be adjusted. When the relay energizes, ancillary contact 'a' closes to connect resistor *R5* as well as potentiometer *R3* to the base of the transistor. The value of *R3* determines the length of the drop-out delay time, which comes into effect after switch S has been opened. Resistor *R5* is a low-value contact protection resistor, which, if the value of *R3* is considerably lower than that of *R2*, ensures that at the instant of pull-on the base voltage cannot fall below that required to hold the relay in an energized condition. This resistor also ensures that the capacitor is always charged to slightly less than the full supply voltage so that the drop-out delay time is independent of the setting of *R2*. Resistor *R6*, which should have a value considerably less than that of *R2*, is included to preclude the possibility of the supply being short-circuited.

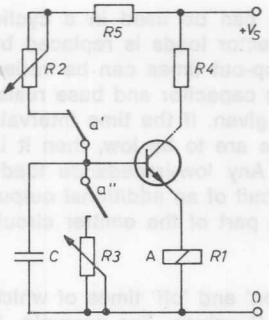
As far as the design and the delay times are concerned, the same rules apply as those given in V. 1. and V. 2.



3. Relay pull-on and drop-out delay circuit

Cyclic Relay Timer

The circuit described in V. 3. can be easily converted to a cyclic timer which permits the contact closing and opening times to be adjusted independently by use of the potentiometer *R3* and *R2* respectively. For given delay times the value of the capacitor can be reduced in inverse proportion to the difference between the energizing and de-energizing voltage of the relay.



4. Cyclic relay timer

V. 5.

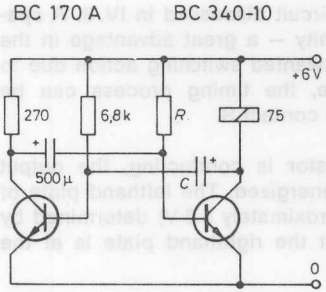
Cyclic Astable Multivibrator Timer

The astable multivibrator discussed in IV. 4. can be used in a cyclic double-timer, if, for example, one of the collector loads is replaced by a relay. In such a circuit the pull-on and drop-out times can be varied within wide limits by variation of the coupling capacitor and base resistor values in accordance with the equations given. If the time intervals involved are long and the capacitance values are to be low, then it is advisable to use a high-impedance circuit. Any low-impedance loads should then be connected in the collector circuit of an additional output transistor, whose base-emitter junction forms part of the emitter circuit of one of the timer transistors.

The circuit shown incorporates a relay, the 'on' and 'off' times of which can be adjusted by variation of the R and C values. For example, if $C = 50\ \mu F$ and $R = 2.7\ k\Omega$, then the 'on' and 'off' times are approximately 0.3 s and 0.1 s respectively.

Because the two time intervals are merely a function of the R and C values, the rather troublesome influence of relay performance on timing, which is a disadvantage of circuits V. 1. to V. 4., has been completely eliminated here. Also, as can be deduced from the equations given in IV. 4., the 'on' and 'off' times are independent of supply voltage variations.

Relay: SEL miniature relay DL 5311 112 (coil resistance 75 Ω)



5. Cyclic astable multivibrator timer

Timer Incorporating Monostable Circuit

This timer is based on the monostable circuit discussed in IV. 3. A special feature of this circuit is noise immunity – a great advantage in the control of plant, for example, because unwanted switching action due to noise is largely eliminated. Furthermore, the timing process can be prematurely interrupted by the opening of contact S.

In the quiescent state, the input transistor is conducting, the output transistor is cut off, and the relay is de-energized. The lefthand plate of the 47 nF capacitor is at a potential (approximately 5.5 V) determined by the 5.6 kΩ / 820 Ω voltage divider, whilst the righthand plate is at the threshold potential of the input transistor.

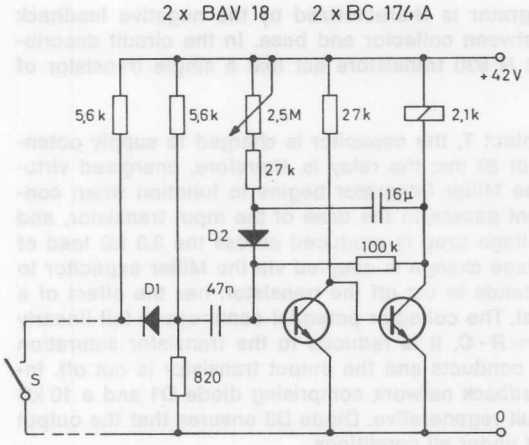
When switch S is closed a negative pulse of approximately 5 V is applied to the base of the input transistor. This causes the transistor to be cut off, the output transistor to be turned on, and the relay to be energized. If switch S is held closed, then the circuit completes its natural timing cycle and flips back into the quiescent state. At the instant of switch-over the base current for the input transistor is supplied by the 16 μF capacitor and then by the supply via the 100 kΩ feedback resistor. The use of this additional resistor ensures that the maximum value to which the timing potentiometer can be set is not restricted by the base current requirements of the input transistor. When the component values shown are used, therefore, the cycling time of the circuit can be varied over the wide range of approximately 0.3 s to 25 s.

If switch S is opened before the monostable has completed its natural cycle, then the positive voltage transient produced at the divider output is coupled, via the 47 nF capacitor, to the base of the input transistor, causing the circuit to return to the quiescent state.

Diode D2 isolates the negative voltage at the 16 μF capacitor plate from the base of the input transistor. It ensures that the transistor base-emitter breakdown voltage cannot be exceeded, and prevents the circuit from being retriggered by the negative trailing edge of the de-energizing transient generated across the relay oil; it also makes possible the interruption of the timing cycle by the opening of switch S.

In the quiescent state diode D1 is reverse biased to approximately 36 V. This means that the amplitude of any noise pulses on the switching line (terminated in 5.6 kΩ) would have to exceed this voltage before the circuit could be random-triggered.

Relay: SEL miniature relay 65, type I 48513 99607 (coil resistance 2.1 kΩ)



6. Timer incorporating monostable circuit

Miller Integrator Timer

A transistor Miller integrator is characterized by the negative feedback capacitor connected between collector and base. In the circuit described the two cascaded 2 N 930 transistors act like a single transistor of very high current gain.

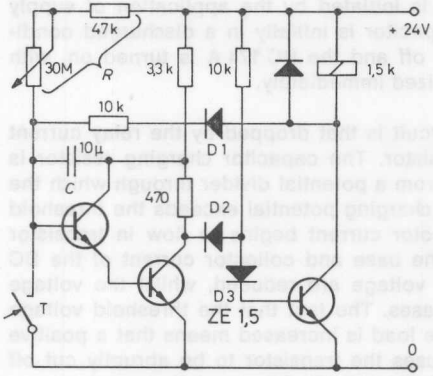
After the closure of contact T, the capacitor is charged to supply potential at a time constant of 33 ms; the relay is, therefore, energized virtually instantaneously. The Miller integrator begins to function when contact T is opened. Current passes to the base of the input transistor, and a linearly increasing voltage drop is produced across the 3.3 kΩ load of this transistor. This voltage change is coupled via the Miller capacitor to the base, and, since it tends to cut off the transistor, has the effect of a negative feedback signal. The collector potential continues to fall linearly until, after a time of $t \approx R \cdot C$, it is reduced to the transistor saturation voltage. Diode D2 now conducts and the output transistor is cut off. Inclusion of a positive feedback network comprising diode D1 and a 10 kΩ resistor makes the circuit regenerative. Diode D3 ensures that the output transistor can be cut off under all conditions.

This circuit differs from the monostable described previously in that it returns to the stable state when the contact is closed, and the timing cycle is started only when this is opened. Furthermore, it is resettable, i. e. whenever contact T is closed the capacitor is charged to supply potential and the timing cycle is restarted.

The circuit may also be used as a relay drop-out delay timer with a maximum delay of 5 minutes.

Relay: SEL Miniature Relay DL 5311 312 (coil resistance 1.5 kΩ)

2x2 N 930 3x BAV 18 BC 171A



7. Miller integrator timer

Timer; Relay Energized During Timing Interval

In this circuit the timing cycle is initiated by the application of supply voltage. Because the timing capacitor is initially in a discharged condition, transistor BC 170 C is cut off and the BC 174 A is turned on, with the result that the relay is energized immediately.

The threshold voltage of the circuit is that dropped by the relay current across the common emitter resistor. The capacitor charging resistor is returned to a potential derived from a potential divider through which the relay current passes. When the charging potential exceeds the threshold voltage, base- and hence collector current begins to flow in transistor BC 170 C, with the result that the base and collector current of the BC 174 A and hence the threshold voltage are reduced, whilst the voltage across the BC 174 A load increases. The fact that the threshold voltage is reduced whilst that across the load is increased means that a positive feedback loop exists, which causes the transistor to be abruptly cut off and the relay to be de-energized. The BC 170 C is now fully turned on.

The circuit remains in this state until the supply voltage is removed. The capacitor now discharges via diode BAV 17 (which provides protection for the BC 170 C) and the base emitter junction of the BC 170 C. This takes several seconds and must be allowed to run its full course, otherwise the next timing cycle would be somewhat shortened.

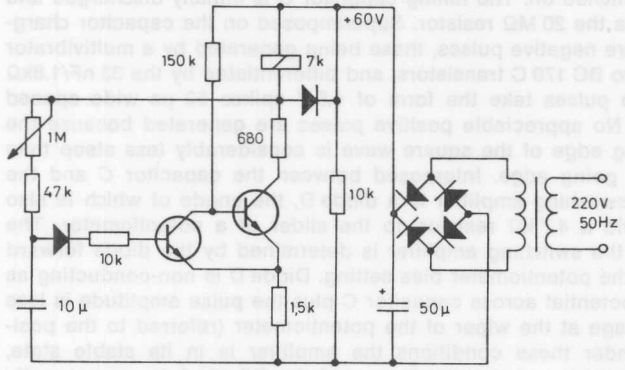
Fig. 8 a shows a two-transistor version of the circuit covering a timing range from 0.5 to 12 s. The three-stage version shown in Fig. 8 b has a timing range of approximately 1 to 160 s. The time for which the circuit is set is virtually unaffected by supply voltage variations.

Relay: SEL HERKON relay HRE 599/1G 48518 89004 (coil resistance 7 kΩ)

Transformer Data

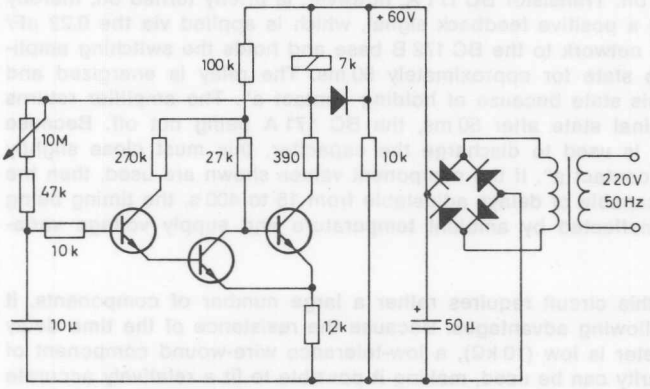
Core: M 42/15.7, laminations IV, alternately stacked
Windings: Primary 5000 turns 0.1 mm dia. en. copper wire
Secondary 1200 turns 0.18 mm dia. en. copper wire

BAV 18 BC 170C BC 174 A BAV 18 B 80 C 600



8 a. 0.5 . . . 12 s timer circuit

2 x BC 172 B BC 174 A BAV 18 B 80 C 600



8 b. 1 . . . 160 s timer circuit

Relay Pull-On Delay Circuit Utilizing Superimposed Pulses

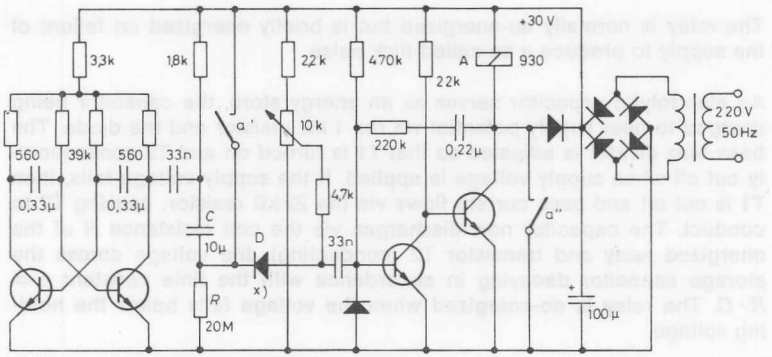
As in the previous circuit, the timing cycle is started when the supply voltage is switched on. The timing capacitor *C* is initially discharged and is charged via the 20 MΩ resistor. Superimposed on the capacitor charging voltage are negative pulses, these being generated by a multivibrator formed by two BC 170 C transistors, and differentiated by the 33 nF/1.8kΩ network. The pulses take the form of 4.5 V spikes 50 µs wide spaced 20 ms apart. No appreciable positive pulses are generated because the positive going edge of the square wave is considerably less steep than the negative going edge. Interposed between the capacitor *C* and the input of the switching amplifier is a diode D, the anode of which is also connected, via a 4.7 kΩ resistor, to the slider of a potentiometer. The threshold of the switching amplifier is determined by the diode forward voltage and the potentiometer bias setting. Diode D is non-conducting as long as the potential across capacitor *C* plus the pulse amplitude is less than the voltage at the wiper of the potentiometer (referred to the positive line). Under these conditions the amplifier is in its stable state, transistor BC 172 B is fully turned on, and the BC 171 A is consequently cut off.

Diode D starts to conduct when the sum of charging voltage and pulse voltage exceeds the diode bias. Negative pulses are then applied, via the 33 nF capacitor, to the base of transistor BC 172 B, which is thus briefly cut off. Transistor BC 171 A, however, is briefly turned on, thereby generating a positive feedback signal, which is applied via the 0.22 µF/220 kΩ *RC* network to the BC 172 B base and holds the switching amplifier in this state for approximately 50 ms. The relay is energized and stays in this state because of holding contact a". The amplifier returns to its original state after 50 ms, the BC 171 A being cut off. Because contact a' is used to discharge the capacitor, this must close slightly later than contact a". If the component values shown are used, then the circuit is capable of delays adjustable from 15 to 400 s, the timing being virtually unaffected by ambient temperature and supply voltage variations.

Although this circuit requires rather a large number of components, it has the following advantages. Because the resistance of the time delay potentiometer is low (10 kΩ), a low-tolerance wire-wound component of good linearity can be used, making it possible to fit a relatively accurate time scale which, if the timer is produced in quantity, needs no individual calibration. In this case it is essential that all the other components are also close-tolerance types.

Because the potentiometer does not form part of a high-resistance timing circuit, it can be fitted separate from the rest of the circuit for remote control purposes. Furthermore, timing could be remote-controlled

2 x BC 170 C BAV 18 BC 172 B BC 171 A BAV 18 B 40 C 600



x) Collector to base diode of a BC 171 with I_R < 1 nA at V_R = 30 V

9. Relay pull-on delay circuit utilizing superimposed pulses

electrically by application of a suitable gating voltage derived from some transducer (or another electronic circuit, for example). In such a remote-control system additional filtering of the control voltage should be provided by means of an *RC* network, in order to remove any impulse noise from the gate diode.

This circuit differs from most conventional timing circuits in that the switching amplifier is capacitively coupled to the *RC* charging circuit rather than directly. Since, once the threshold has been exceeded, the charging capacitor has to supply energy to the switching amplifier only during the 'spike-on' periods, the time constant of the charging circuit can be made many times longer than would be possible with direct coupling, the increase being roughly inversely proportional to the pulse duty factor. The circuit is therefore particularly suitable for long timing cycles. With suitable components delay times up to 3600 s (= 1 h) can be attained. For example:
$R = 100\ \text{M}\Omega$
$C = 22\ \mu\text{F}$, when $\tau_C > 10^5$ s at $T_{amb} = 25\ ^\circ\text{C}$
Gate diode: Silicon diode with $I_R < 0.1$ nA at $V_R = 30$ V
and $T_{amb} = 25\ ^\circ\text{C}$

Relay: SEL Miniature Relay 54 Type 104.250 (coil resistance 930 Ω)

Transformer Data

Core: M 42/15.7, laminations IV, alternately stacked
Windings: Primary 5000 turns 0.10 mm dia. en. copper wire
Secondary 600 turns 0.20 mm dia. en. copper wire

Flick Pulse Relay

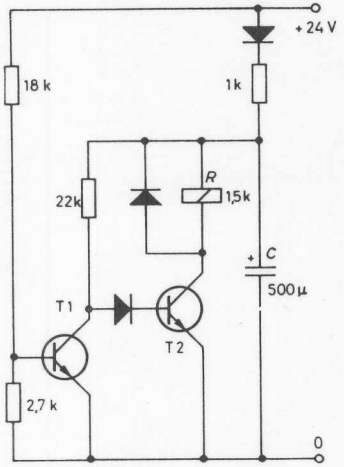
The relay is normally de-energized but is briefly energized on failure of the supply to produce a so-called flick pulse.

An electrolytic capacitor serves as an energy store, the capacitor being charged to near supply potential via the 1 kΩ resistor and the diode. The base-bias divider is adjusted so that T1 is turned on and T2 consequently cut off when supply voltage is applied. If the supply voltage fails, then T1 is cut off and base current flows via the 22 kΩ resistor, causing T2 to conduct. The capacitor now discharges via the coil resistance R of the energized relay and transistor T2 (conducting), the voltage across the storage capacitor decaying in accordance with the time constant $\tau = R \cdot C$. The relay is de-energized when the voltage falls below the holding voltage.

The circuit shown produces a 0.5 s flick pulse; it consumes initially 25 mA (when the storage capacitor is being charged) and then 2 mA.

Relay: SEL Miniature Relay DL 5311 312 (coil resistance 1.5 kΩ)

3 x BAV 18 2 x BC 171 B



10. Flick pulse relay

VI. Control Circuits

Contents

AC Transistor Switch

Transistors are, in general, considered unsuitable for AC switching, thyristors normally being employed for this purpose. This requires, however, two thyristors, one to conduct during the positive and one to conduct during the negative half-cycle; also the triggering of two inverse-parallel connected thyristors sometimes presents problems.

The simple circuit shown below allows an AC load to be switched by means of a transistor via a bridge rectifier. The transistor is connected to the DC terminals, and the load R_L, through which the alternating current passes, is connected to the AC terminals of the bridge rectifier. Depending on the current gain of the transistor, the following approximate drive voltage is required to energize the load:

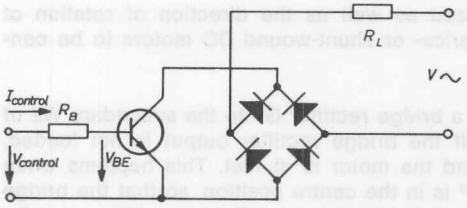
$$V_{control} \approx \frac{\sqrt{2} \cdot V\sim \cdot R_B}{h_{FE} \cdot R_L} + V_{BE}$$

where V_{BE} is approximately 0.7 V and the value of R_B, the base resistor, is chosen so that a voltage of approximately 0.7 V is dropped across it. If the circuit is current driven, then this current $I_{control}$ should be approximately

$$I_{control} \approx \frac{\sqrt{2} \cdot V\sim}{h_{FE} \cdot R_L}$$

A worst case h_{FE}-value just within the lower spread limit should be assumed.

The transistor must be rated for a collector-emitter voltage in excess of the peak value of the alternating voltage to be switched.



1. AC Transistor switch

DC Motor Control Circuit

This circuit permits the speed as well as the direction of rotation of small permanent magnet, series- or shunt-wound DC motors to be continuously varied.

The motor is connected via a bridge rectifier G1 to the secondary W2 of an AC power transformer. If the bridge rectifier output is not loaded, then no current is drawn and the motor is at rest. This happens when the wiper of potentiometer P is in the centre position, so that the bridge formed by resistors *R1, R2* and potentiometer P is at balance; under these conditions the base-emitter voltage of the transistor is zero and no collector current can flow. If the wiper of P is moved away from the centre position, then the transistor conducts either during each positive or during each negative half-cycle of the voltage across W2, depending on the direction in which P is turned. The motor current therefore passes either via D1 and D2, for rotation in one direction, or via D3 and D4 for rotation in the reverse direction. Thus, the motor is supplied with a unidirectional half-wave current whose amplitude and direction of flow depends on the position of the wiper of P. In this way a permanent magnet motor can be controlled to run in either direction.

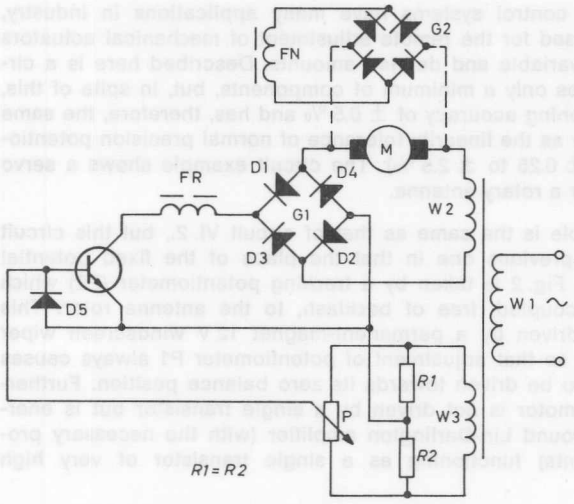
In the case of a series-wound motor, the field winding FR should be connected in series with the collector of the transistor so that the field current always passes in the same direction. In the case of a permanent or shunt-wound motor the collector of the transistor should be directly connected to the rectifier.

The field winding FN of shunt-wound motors must be connected in parallel with the rotor via a second bridge rectifier to ensure that the field current can flow in one direction only. Diode D5 prevents the application of excessive reverse voltage to the transistor base-emitter junction.

Design Notes

Non-essential components such as interference suppression capacitors, freewheel diodes, etc., which are sometimes required, have been omitted from the circuit for the sake of clarity.

Because the motor is energized by unsmoothed (i. e. half-wave) DC, the RMS value of the AC voltage across W3 necessary to attain full power should be approximately 1.5 times the rated motor voltage. Similarly the cross section of the wire used for winding W2 should be chosen so as to accomodate 1.5 times the rated motor current.



2. DC Motor control circuit

The transistor should have the following maximum ratings:

Collector-emitter voltage $V_{CE\,max} > 1.5\,V_{rms\,W2}$
Collector current $I_{C\,max} > 1.5\,I_{mot\,start}$ (= motor starting current)
Dissipation $P_{max} > 0.5 \cdot V_{rms} \cdot I_{mot\,start}$

Rectifier G1 must be capable of handling the voltage across W2 and the motor starting current, whilst rectifier G2 must be capable of handling the voltage across W2 and the current through the field winding FN. Drive voltage winding W3 should supply approximately 6 to 30 V, and the values of *R1*, *R2* and P should be chosen accordingly. Circuit conditions must be such that the half-wave voltage obtained with the wiper in one of the extreme positions is high enough to drive the transistor into saturation. The higher the current gain of the transistor is, the higher the values of *R1*, *R2* and P can be made. Therefore, rather than employ a single transistor it may be advantageous to use several transistors in a Lin or Darlington circuit.

Servo Control System

Electronic servo control systems have many applications in industry, where they are used for the remote adjustment of mechanical actuators by continuously variable and defined amounts. Described here is a circuit which requires only a minimum of components, but, in spite of this, provides a positioning accuracy of ± 0.5 % and has, therefore, the same order of accuracy as the linearity tolerance of normal precision potentiometers (usually ± 0.25 to ± 2.5 %). The circuit example shows a servo control system for a rotary antenna.

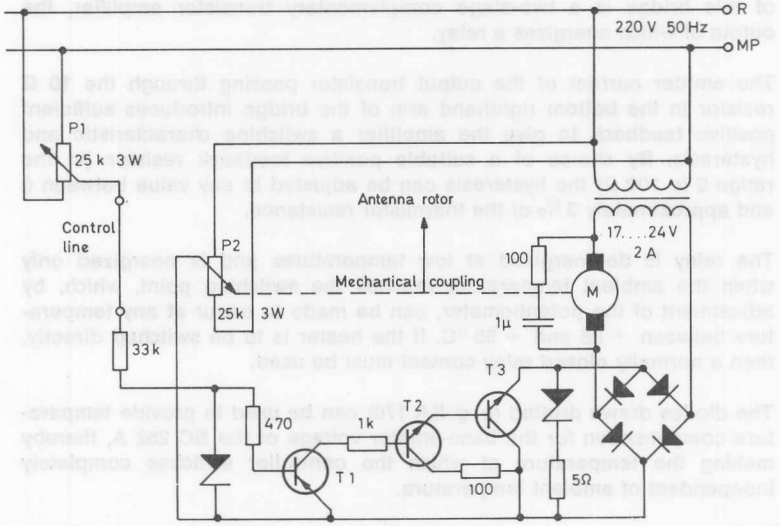
The basic principle is the same as that of circuit VI. 2., but this circuit differs from the previous one in that the place of the fixed potential divider *R1*, *R2* in Fig. 2 is taken by a tracking potentiometer (P2) which is mechanically coupled, free of backlash, to the antenna rotor. This rotor is in turn driven by a permanent-magnet 12 V windscreen wiper motor connected so that adjustment of potentiometer P1 always causes the wiper of P2 to be driven towards its zero balance position. Furthermore, the servo motor is not driven by a single transistor but is energized by a compound Lin-Darlington amplifier (with the necessary protective components) functioning as a single transistor of very high current gain.

Since the base-emitter threshold voltage of T1 causes the servo amplifier to be inoperative at input voltages below approximately 0.6 V, the servo system exhibits a hysteresis effect, which, however, is less pronounced at high bridge supply voltages. Therefore, in the example shown, in order to make the circuit as simple as possible, the bridge is energized directly from the 220 V AC line, with the additional advantage that only one control line is required. If suitable filter networks are introduced, then this control line could be the inner conductor of the coaxial antenna feeder. The effect of any capacitance between the control line and ground (up to 10 nF for 100 m of cable) can be nullified by connecting a capacitor of equal value from the slider of P2 to ground. Any tendency towards overshoot is best eliminated by using a high step-down ratio between motor and antenna rotor. If the bridge is powered directly from the AC line (as shown here), then it is essential that the wiring complies with local safety regulations. Note that it is considerably safer to energize the bridge via an isolation transformer and thus eliminate the risk of electric shock.

Hysteresis and bridge supply voltage are related as follows:

Bridge Supply Voltage V_{rms}	Hysteresis (% of P1 Max. Angle of Rotation)
50 V	1.2 %
100 V	0.6 %
220 V	0.3 %

ZPD 5,6 BC 251 B BC 340-10 2 N 3055 ZU 39 B40 C 3200 - 2200



3. Servo control system

The two potentiometers need not necessarily be of the same value, and can be of different values from those shown in the circuit. However, the dissipation sets a lower limit of approximately 5 kΩ, and the risk of noise pick-up on the control line an upper limit of approximately 100 kΩ.

Zener diode ZU 39 limits to a safe value any induced motor voltages, which, without this diode, could exceed the maximum permissible collector-emitter voltage of transistor T3.

If a low-power servo motor is used, then a transistor type BD 106 can be employed for T3. Since the motor is to be energized by unsmoothed DC, the RMS value of the alternating energizing voltage should be 1.5 to 2 times the rated motor voltage. The cross-section of the transformer secondary wire however, need only accomodate the rated current, because the system will only be operated intermittently.

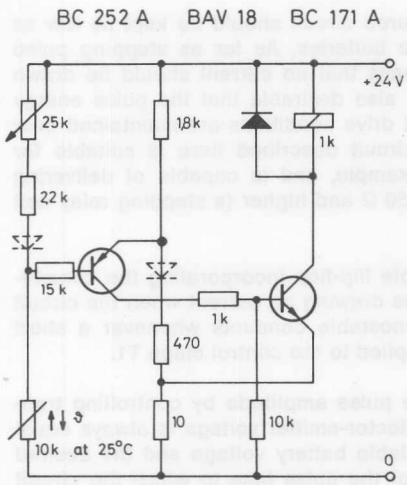
On-Off Temperature Controller

The temperature is sensed by means of a thermistor (NTC) connected in one arm of a Wheatstone bridge. Connected to the "detector" terminals of this bridge is a two-stage complementary transistor amplifier, the output of which energizes a relay.

The emitter current of the output transistor passing through the 10 Ω resistor in the bottom righthand arm of the bridge introduces sufficient positive feedback to give the amplifier a switching characteristic and hysteresis. By choice of a suitable positive feedback resistor (in the range 0 to 100 Ω) the hysteresis can be adjusted to any value between 0 and approximately 3 % of the thermistor resistance.

The relay is de-energized at low temperatures and is energized only when the ambient temperature reaches the switching point, which, by adjustment of the potentiometer, can be made to occur at any temperature between + 35 and + 95 °C. If the heater is to be switched directly, then a normally closed relay contact must be used.

The diodes drawn drotted (e. g. BA 170) can be used to provide temperature compensation for the base-emitter voltage of the BC 252 A, thereby making the temperature at which the controller switches completely independent of ambient temperature.



4. On-off temperature controller

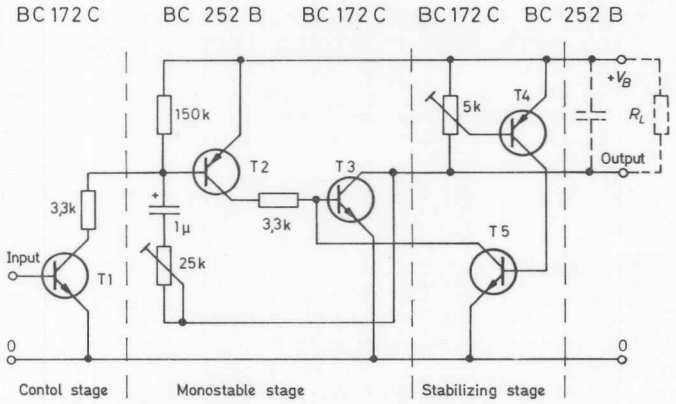
Stabilized Stepping Pulse Generator

The consumption of a battery-powered circuit should be kept as low as possible to prolong the life of the batteries. As far as stepping pulse generators are concerned, this means that no current should be drawn during the 'pulse-off' periods. It is also desirable that the pulse energy be stabilized in order that constant drive conditions are maintained over the full life of the battery. The circuit described here is suitable for energizing stepping motors, for example, and is capable of delivering 25 ms drive pulses into a load of 250 Ω and higher (a stepping relay coil or similar, for example).

The circuit is basically a monostable flip-flop incorporating the complementary transistors T2 and T3, these drawing no current when the circuit is in the quiescent state. The monostable conducts whenever a short pulse of 1 ms duration or less is applied to the control stage T1.

Transistors T4 and T5 stabilize the pulse amplitude by controlling transistor T3 in such a way that its collector-emitter voltage is always equal to the difference between the available battery voltage and the desired pulse amplitude. After the elapse of the pulse time to which the circuit has been set, all transistors return to the non-conducting state.

The stabilization of the output pulse amplitude against battery voltage variations has the additional advantage of keeping the width of the pulses, produced by the monostable, constant; this is because the capacitor in the 25 kΩ / 1 μF *RC* timing network, to which the output pulses derived from T3 collector are applied, is always recharged to the same potential. For example, without stabilization a battery voltage reduction from 1.8 V to 1.2 V would cause the width of the output switching pulse to be shortened by 20 %, whereas with the stabilizing circuit the pulse width is held constant within 1 to 2 %.



5. Stabilized stepping pulse generator

VII. Metering and Monitor Circuits

Contents

Revolution Counter for Motor Vehicles

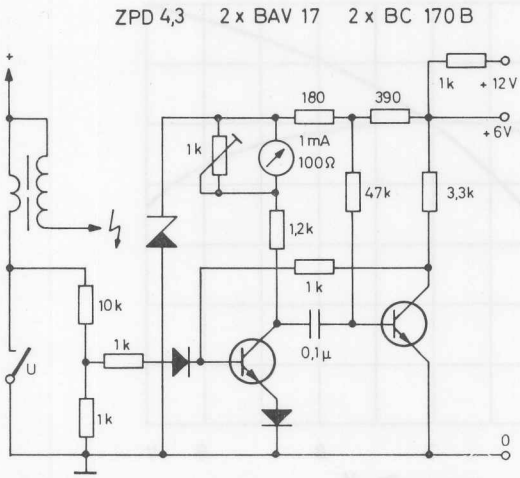
In this electronic tachometer circuit current pulses of constant waveform at a repetition frequency proportional to the engine speed are passed through a meter which, because of its inertia, acts as an integrator.

A pulse sequence at a frequency proportional to engine speed can be derived from the engine contact breaker U, but the duration of these pulses is by no means constant and varies with contact breaker adjustment as well as engine speed. Therefore, the pulses must be suitably shaped before they can be passed through the meter, this being accomplished by the use of a monostable multivibrator, as shown in Fig. 1a.

In the quiescent state the righthand transistor conducts, Whenever the contact breaker opens a positive pulse is applied to the base of the lefthand transistor, causing the monostable to change to the metastable state. The pulses generated in this way are averaged in the meter connected in the collector circuit of the lefthand transistor. Thus an indication of engine speed is obtained which is largely unaffected by the shape of the contact breaker pulses. The lefthand transistor conducts for approximately 3.5 ms – long enough to allow any transients generated during the ignition and extinction of the sparks to die down without causing the monostable to be triggered several times during each engine stroke, but short enough to permit frequencies up to 250 Hz and more (250 Hz $\triangleq$ 7500 RPM of a four-cylinder four-stroke engine) to be measured.

A diode connected in the emitter circuit of the lefthand transistor ensures that the meter readings are unaffected over a wide range of temperatures; it compensates for and tracks any threshold voltage variations of the righthand transistor due to temperature variations. Without this diode, a temperature increase would cause the threshold voltage, and hence off-time of this transistor, to decrease with a correspondent reduction in meter reading. The compensating diode keeps any errors due to temperature increases up to 50 °C within less than + 1 %.

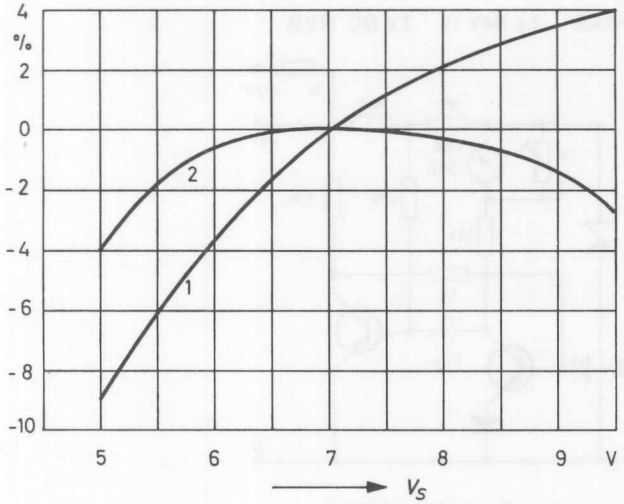
Particular trouble has been taken to ensure that supply voltage variations have no effect on the meter reading. Because the output voltage of a nominal 6 V vehicle supply system can vary between 6 and 8 V, depending on the state of the battery, adjustment of the voltage regulator, generator speed and the effective load, supply stabilization is essential if the accuracy of speed indication is to be independent of vehicle supply voltage. One might think that the simplest way to achieve this is to stabilize the entire supply by means of a zener diode, but this method is not entirely satisfactory because zener diodes of the required low operating voltage have a relatively high incremental resistance. In the curve 1 in Fig. 1b. the variation in speed indication still remaining



1 a. Revolution counter for motor vehicles

is plotted as a function of unstabilized supply voltage for a circuit stabilized by a zener diode ZPD 4.3.

Considerably better results are obtained if only the collector voltage of the lefthand transistor is stabilized by means of a zener diode and series resistor. In this case the base bias for the righthand transistor is tapped off the zener diode series resistor whilst the transistor load is connected to the unstabilized supply. Because of imperfect stabilization the meter current still tends to increase slightly with supply voltage, but, at the same time, the capacitor, which determines the on-time of the lefthand transistor, is discharged more rapidly via the 47 kΩ resistor, because this is now returned to a point of higher potential. The result is that the on-time tends to become shorter as the supply voltage is increased, making the meter indication, which is proportional to the product of the lefthand transistor collector current and the on-time, virtually independent of supply voltage variations over a certain range (curve 2). Initially there is a fairly rapid increase in meter indication as the supply voltage is varied, pointing to the fact that under these conditions the current increase is still not nullified by the effect of 'on-time' reduction. As the supply voltage is further increased the rate of on-time decrease is



1 b. Speed indication error as a function of supply voltage

greater than the rate at which the current increases, and the change in meter indication is reduced accordingly. The result is that a variation of supply voltage from 6 to 8 V causes an error of not more than 0.5 % – an error which would have been approximately 5.5 % (curve 1) if the entire supply had been stabilized.

The same circuit can also be used for vehicles with a 12 V system if a 1 kΩ dropping resistor is used; the error in the range 11 . . . 17 V is then less than 0.5 %.

Frequency Meter

This circuit gives a direct indication of input frequency on a moving coil meter, and also produces a frequency-proportional DC output, which could be used as the X-deflection signal for an X/Y plotter. The measurement range is from 10 Hz to 1 MHz.

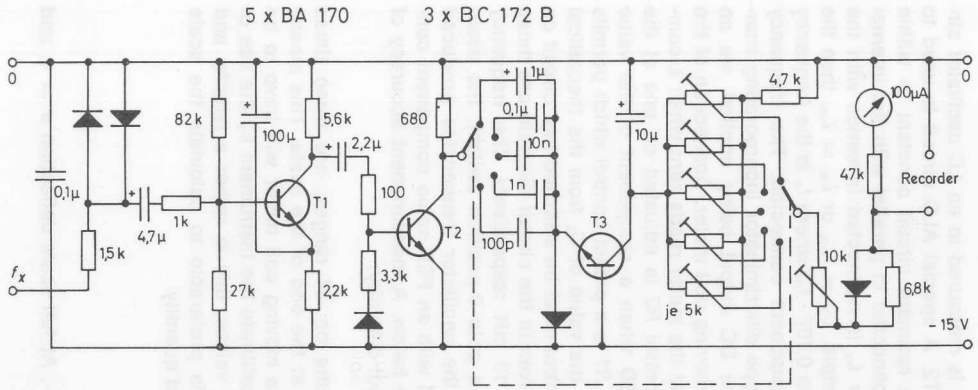
The input signal is at first clipped by two inverse-parallel connected diodes. Transistor T1 functions as a pre-amplifier, transistor T2 as an amplifier/limiter, and transistor T3 as a discriminator/counter. During the time when T2 is cut off, capacitor *C* (selected by means of the range switch) is charged. When T2 is turned on, capacitor *C* discharges via T3. The average collector current of T3 is proportional to the input signal frequency, and the voltage dropped across R_C, the collector load of T3, is

$$V \approx C \cdot R_C \cdot f \cdot V_B.$$

The collector load of T3 consists of a fixed resistor in series with switch-selected preset controls; these are used to set the meter indication to the correct value at the centre frequency of each range, i. e. at 50 Hz, 500 Hz, 5 kHz, etc., and make it possible for timing capacitors with a tolerance of ± 10 % to be used. Because supply voltage variations directly affect the measurement result, the supply voltage must be stabilized.

The 10 kΩ potentiometer is included to permit the meter indication to be corrected in accordance with any supply voltage in the range 14 . . . 16 V. The frequency meter has the following performance specification:

Current consumption		18 mA at FSD
Required input level	Ranges 1 . . . 4:	> 70 mV
	Range 5:	> 350 mV
Input impedance		> 1.5 kΩ
Accuracy	Ranges 1 . . . 4:	< ± 2 % of FSD
	Range 5:	< ± 3 % of FSD
Frequency ranges	(1) 0 . . . 100 Hz	
	(2) 0 . . . 1000 Hz	
	(3) 0 . . . 10 kHz	
	(4) 0 . . . 100 kHz	
	(5) 0 . . . 1 MHz	
Recorder output	5 V across 50 kΩ at FSD	



2. Frequency meter

Direct-Reading *LC*-Meter

The unknown capacitor or inductor is measured in an *LC* oscillator circuit formed by transistors T1 and T2. A special ALC circuit is used to hold the signal voltage across the resonant circuit constant to within 30 to 40 mV. If a capacitor C_x is connected in parallel with the internal tuning capacitor C_o, or an inductor L_x is connected in series with the internal inductor L_o, and if, for example, $C_x = C_o$, or $L_x = L_o$, then the frequency of oscillation is reduced to $0.707 \cdot f_o$, where f_o is the frequency produced without the unknown component connected. The frequency change is measured by a counter type discriminator incorporating transistors T3 and T4, the discriminator DC output being applied, via an emitter follower formed by T5, to a moving coil meter. Connection of the meter in a bridge circuit ensures that the meter reads zero when a component is not connected. Preset control *R2* is adjusted on one of the ranges so that the meter reads FSD when a component of the value $C_x = C_o$ (or $L_x = L_o$) is connected. *R1* is a preset control which permits compensation for any difference in the value of C_L from the theoretical value; thus a different *R1* preset control must be switched into circuit on each range. The C_o and L_o values given in the circuit diagram are those required for an FSD of 10 nF or 10 mH respectively. The frequency ranges (selectable by means of a 4 pole 9-position switch), the associated L_o, C_o and C_L values and the oscillator frequencies produced without the test item connected and with an FSD value component connected are summarized in the table below. A measurement accuracy of ± 3 % of FSD can be attained without difficulty.

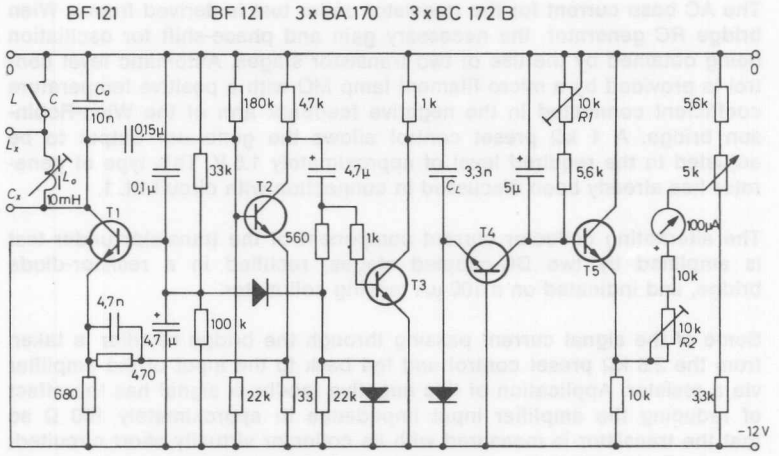
The scale points, although the same on all ranges, are three times farther apart at the beginning than at the end of the scale. This means that the normally linear scale of the moving coil meter will have to be redrawn. Although it is possible to calibrate the instrument by the use of inductors and capacitors of known values, this is rather a lengthy and not very accurate method, and it is preferable to calculate the scale points. For this purpose a normalized quantity

$$f_{rel} = \frac{f_x}{f_o} = \frac{1}{\sqrt{1+a}}$$

is introduced, where $a = \frac{L_x}{L_o}$ or $\frac{C_x}{C_o}$. At full scale deflection $a = 1$, and hence

$$f_{rel} = \frac{1}{\sqrt{2}} \approx 0.707$$

To determine the scale shape, a table should be prepared in which the relative frequencies f_{rel} are listed for as many a values in the 0.01 to 1 range as required; the values for $1 - f_{rel}$ should also be listed in a second column. This is needed because the scale shape equation is



3. Direct-reading *LC*-meter

$$n = \frac{(1 - f_{rel})\, n_{max}}{1 - f_{rel\ min}}$$

where $f_{rel\ min}$ is the lowest relative frequency (this is produced when $a = 1$, i. e. $f_{rel} = 0.707$). The letter n stands for the number of scale divisions to which the pointer is deflected at f_{rel} after the instrument has been adjusted to read n_{max} (= FSD) at $f_{rel\ min}$. All this assumes that the meter itself has a linear scale law.

Range No.	FSD	L_o mH	C_o nF	C_L nF	f_o kHz	f_x at $C_x = C_o$ or at $L_x = L_o$ kHz
1	100 pF	1	0.1	0.1	502	355
2	1 nF	1	1	0.33	158	112
3	10 nF	10	10	3.3	15.8	11.2
4	100 nF	10	100	10	5.02	3.55
5	10 µH	0.01	10	0.1	502	355
6	100 µH	0.1	10	0.33	158	112
7	1 mH	1	10	1	50.2	35.5
8	10 mH	10	10	3.3	15.8	11.2
9	100 mH	100	10	3.3	5.02	3.55

Direct-Reading Transistor β-Meter

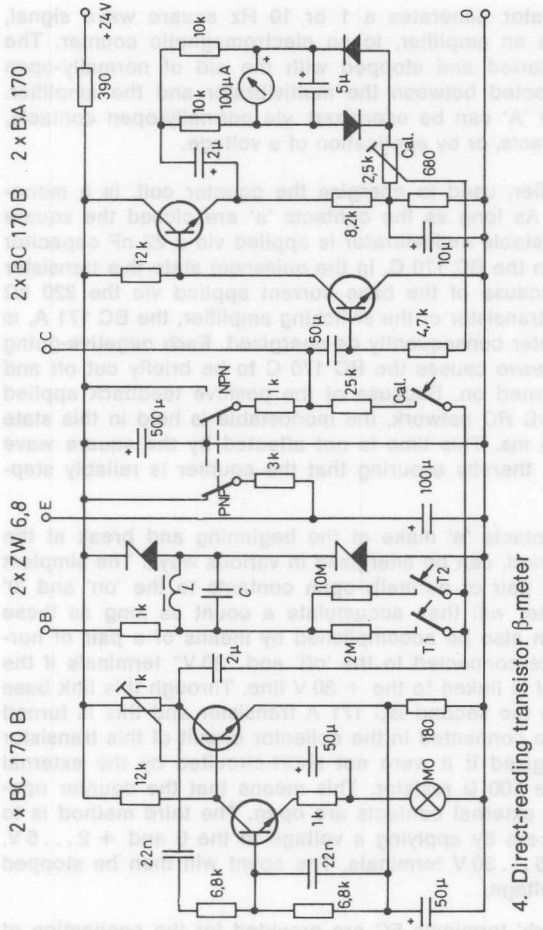
The AC base current for the transistor under test is derived from a Wien bridge *RC* generator, the necessary gain and phase-shift for oscillation being obtained by the use of two transistor stages. Automatic level control is provided by a micro filament lamp MO with a positive temperature coefficient connected in the negative feedback arm of the Wien-Robinson bridge. A 1 kΩ preset control allows the generator output to be adjusted to the required level of approximately 1.5 V. This type of generator has already been discussed in connection with circuit III. 1.

The alternating collector current component of the transistor under test is amplified by two DC-coupled stages, rectified in a resistor-diode bridge, and indicated on a 100 μA moving coil meter.

Some of the signal current passing through the bridge rectifier is taken from the 2.5 kΩ preset control and fed back to the input of the amplifier via a resistor. Application of this negative feedback signal has the effect of reducing the amplifier input impedance to approximately 100 Ω so that the transistor is measured with its collector virtually short circuited; also it largely eliminates the effect of diode non-linearity on the meter indication, allowing the use of silicon diodes in the bridge rectifier despite the low output level of only 3 V_{pp}.

The AF generator and metering amplifier operate from a 13.5 V supply, stabilized by use of two ZW 6.8 zener diodes. The base of the transistor under test is DC-connected, via the coil of a tuned rejection circuit and a protection resistor, to the junction of the two zener diodes. The rejection circuit has a dynamic resistance of more than 1 MΩ at 1 kHz. Because the 100 μF emitter capacitor is charged via the base-emitter junction of the transistor under test, a protective 1 kΩ base current limiting resistor is included.

The emitter current of the test item is largely determined by the value of the emitter resistor and is approximately 2 mA. Because there is a voltage drop across the 1 kΩ collector load, the collector-base voltage is approximately 5 V. For transistor measurements, the test signal is applied to the base via either a 2 MΩ resistor switched by T1 (β = 0...100), or a 20 MΩ resistor switched by T2 (β = 0...500). Push-button switch T3 is used for test and calibration purposes; it connects the input of the metering amplifier via a 25 kΩ resistor directly to the generator. The 2.5 kΩ preset control is then used to adjust the gain of the metering amplifier so that a meter deflection of 80 % of FSD is produced. The circuit arrangement is such that the 1 kΩ resistor, which normally forms the test item collector load, remains connected to the metering amplifier so it cannot falsify the test result.



4. Direct-reading transistor β-meter

Coil Data

Core: Ferrite cup core 59 mm dia. x 36 mm, with air gap, $A_L = 1000\ \mu H/turns^2$

Winding: 1550 turns 0.2 mm dia. en. copper wire

Event Timer

An astable multivibrator generates a 1 or 10 Hz square wave signal, which is applied, via an amplifier, to an electromagnetic counter. The timing process is started and stopped with the aid of normally-open relay contacts connected between the multivibrator and the amplifier. The associated relay 'A' can be energized, via normally-open contacts, normally-closed contacts, or by application of a voltage.

The switching amplifier, used to energize the counter coil, is a monostable multivibrator. As long as the contacts 'a' are closed the square wave output of the astable multivibrator is applied via a 22 nF capacitor and a 1 kΩ resistor to the BC 170 C. In the quiescent state this transistor is fully saturated because of the base current applied via the 220 kΩ resistor; the second transistor of the switching amplifier, the BC 171 A, is cut off, and the counter consequently de-energized. Each negative-going edge of the square wave causes the BC 170 C to be briefly cut off and the BC 171 to be turned on. Because of the positive feedback applied via the 0.22 µF / 68 kΩ *RC* network, the monostable is held in this state for approximately 25 ms. This time is not affected by the square wave repetition frequency, thereby ensuring that the counter is reliably stepped on.

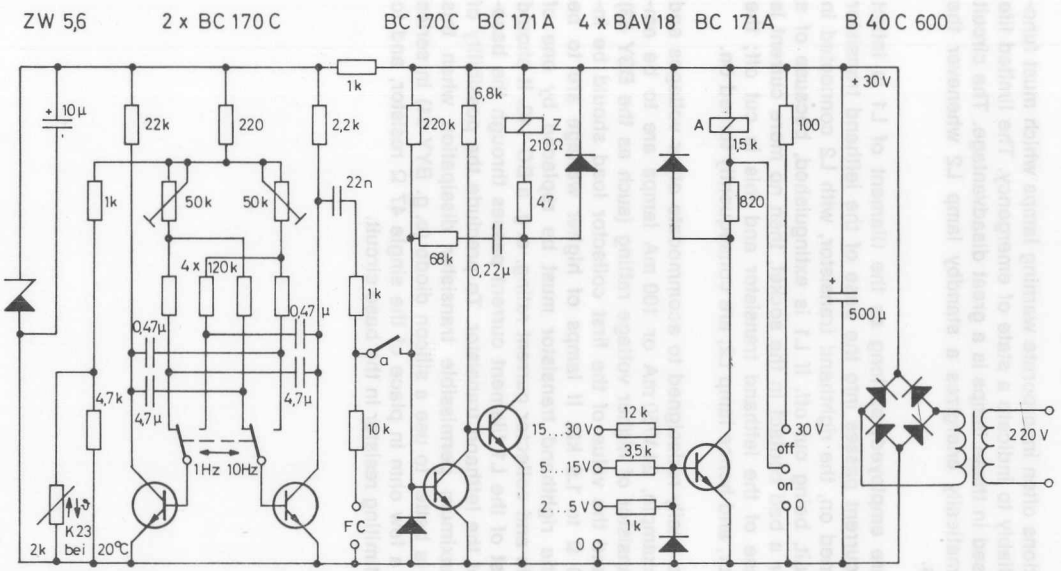
Relay 'A', whose contacts 'a' make at the beginning and break at the end of the timing period, can be energized in various ways. The simplest way is to connect a pair of normally-open contacts to the 'on' and '0' terminals. The counter will then accumulate a count as long as these stay closed. This can also be accomplished by means of a pair of normally-closed contacts connected to the 'off' and "30 V" terminals if the "15 . . . 30 V" terminal is linked to the + 30 V line. Through this link base current is applied to the second BC 171 A transistor and this is turned on. Relay 'A' which is connected in the collector circuit of this transistor would then be energized if it were not short-circuited by the external n. c. contacts via the 100 Ω resistor. This means that the counter operates as long as the external contacts are open. The third method is to start the timing process by applying a voltage to the 0 and + 2 . . . 5 V, + 5 . . . 15 V, or + 15 . . . 30 V terminals. The count will then be stopped on removal of this voltage.

The 'Frequency Check' terminals FC are provided for the connection of an oscilloscope, frequency meter or counter.

Relay: SEL miniature relay DL 5311 312 (coil resistance 1.5 kΩ)
Counter: Hengstler FO43A, 24 V DC; 25 p.p.s. max. (coil resistance 210 Ω)

Transformer Data

Core: M 55/21, lamination IV, alternately stacked
Windings: Primary 2500 turns 0.15 mm dia. en. copper wire
Secondary 290 turns 0.30 mm dia. en. copper wire



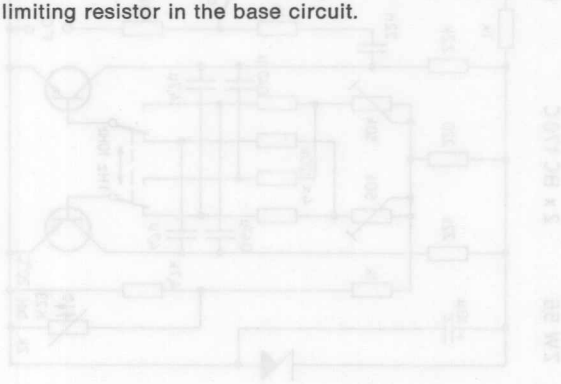
5. Event timer

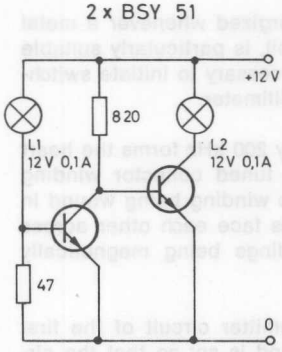
Energizing Circuit for Standby Warning Lamp

Technical installations often incorporate warning lamps which must function absolutely reliably to indicate a state of emergency. The limited life of the filaments used in these lamps is a great disadvantage. The circuit shown here automatically energizes a standby lamp L2 whenever the main lamp L1 fails.

Two transistors are employed; as long as the filament of L1 is intact part of the lamp current passes into the base of the lefthand transistor so that this is turned on, the righthand transistor, with L2 connected in the collector circuit, being cut off. If L1 is extinguished, because of a broken filament or a bad contact in the socket, then no more current is passed to the base of the lefthand transistor and this is cut off; the righthand transistor, and hence lamp L2, are consequently turned on.

The circuit can be easily redesigned to acommodate other voltages and currents. If, for example, 24 V/50 mA or 100 mA lamps are to be employed, then a transistor of higher voltage ratting (such as the BSY 53) should be used and the value of the first collector load should be increased from 820 Ω to 1.5 kΩ. If lamps of higher wattage are to be employed, then the righthand transistor must be replaced by one of higher current gain and collector current rating, e. g. a BC 140. It should be noted that most of the L1 filament current passes through the base-emitter junction of the lefthand transistor. To preclude the possibility of exceeding the maximum permissible transistor dissipation when this current is high, it is better to use a silicon diode (e. g. BYY 31) in series with a resistor of a few ohm in place of the single 47 Ω resistor, and to include a current limiting resistor in the base circuit.





6. Energizing circuit for standby warning lamp

Inductive Limit Switch

This circuit, which causes a relay to be de-energized whenever a metal strip is inserted between the two halves of a coil, is particularly suitable for use as a limit switch. The insertion depth necessary to initiate switching action can be set to within a fraction of a millimeter.

A Meißner oscillator oscillating at approximately 200 kHz forms the heart of the circuit. The oscillator coil is split, the tuned collector winding being wound in one half and the feedback base winding being wound in the other half of a ferrite cup core. Both halves face each other across a gap of approximately 5 mm, the two windings being magnetically coupled across this gap.

The variable 1 kΩ resistor connected in the emitter circuit of the first transistor introduces local negative feedback and is set so that the circuit just oscillates. If a metal strip is inserted between the two halves of the coil, then the eddy currents induced in the strip reduce the magnetic flux and hence the positive feedback signal to such an extent that the oscillations cease.

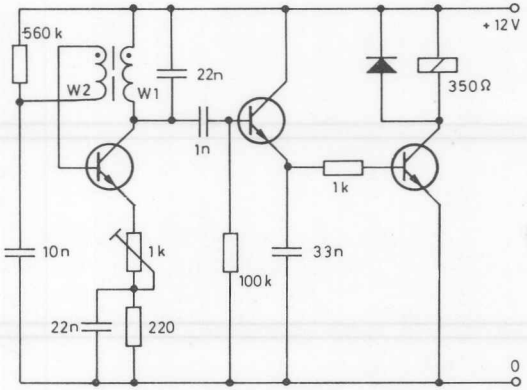
From the collector, the oscillator signal is coupled, via a 1 nF capacitor, to a common collector stage where it is rectified. When the circuit oscillates a direct voltage is developed across the emitter-reservoir capacitor in this stage. This voltage is applied to the base of the output transistor, which is thus turned on; the relay is then energized, and is de-energized only when the oscillations cease.

Relay: SEL miniature relay DL 5311 212 (coil resistance 350 Ω)

Coil Data

Core: Ferrite cup core 11 mm dia. x 7 mm
Windings: W1 = 40 turns 0.12 mm dia. en. copper wire
W2 = 75 turns 0.12 mm dia. en. copper wire

3 x BC 170 C BA 170



7. Inductive limit switch